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(54) QUANTUM DOT DEVICES

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(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(21) Appl. No.: **18/311,582**

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Related U.S. Application Data

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(60) Provisional application No. 62/417,047, filed on Nov. 3, 2016.

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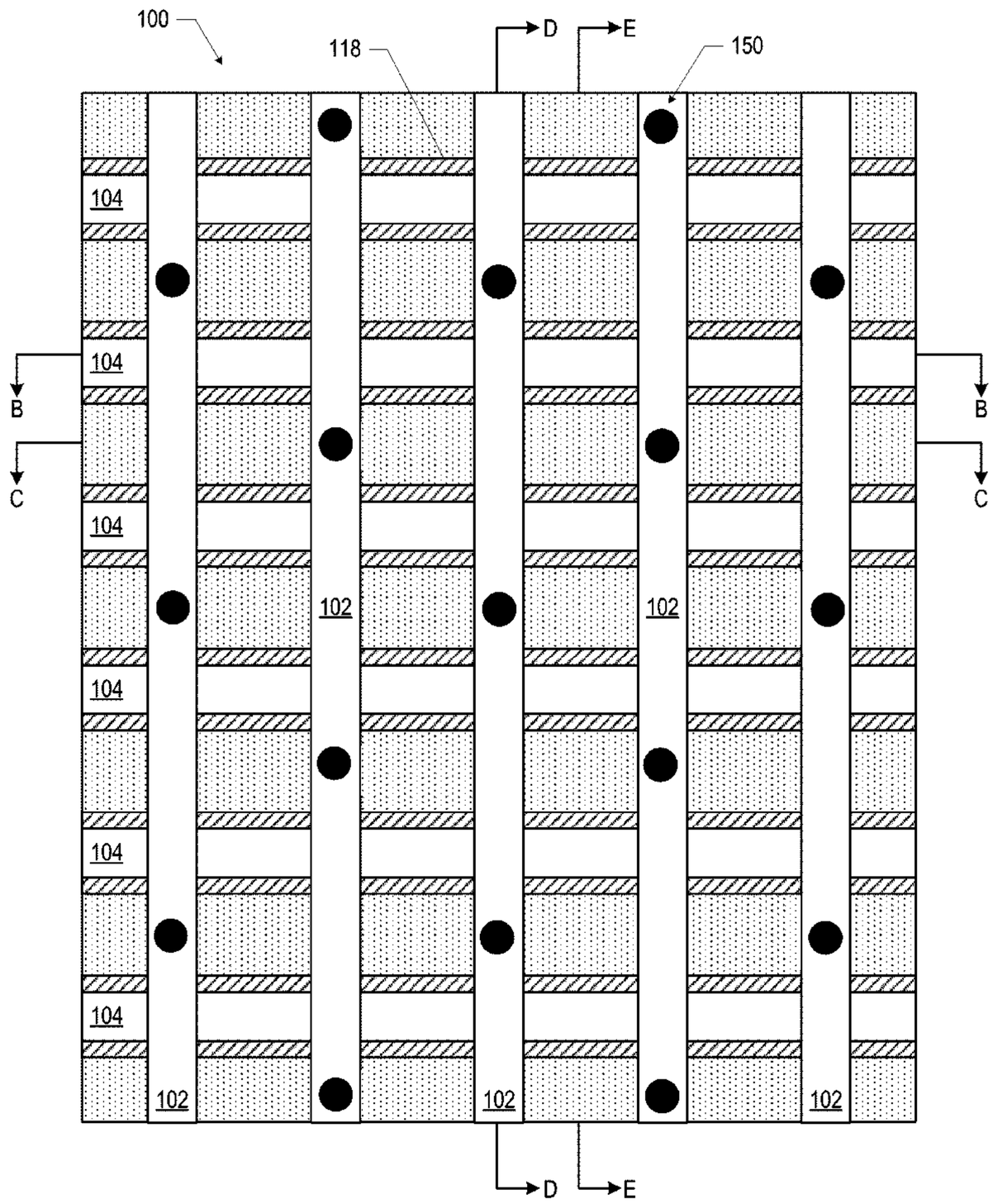
H01L 21/8234	(2006.01)
H01L 29/66	(2006.01)
H01L 29/778	(2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/088*** (2013.01); ***G06N 10/00*** (2019.01); ***H01L 21/823456*** (2013.01); ***H01L 29/66977*** (2013.01); ***H01L 29/778*** (2013.01); ***H10N 69/00*** (2023.02); *B82Y 10/00* (2013.01)

(57) **ABSTRACT**

Quantum dot devices, and related systems and methods, are disclosed herein. In some embodiments, a quantum dot device may include a quantum well stack; a plurality of first gates above the quantum well stack; and a plurality of second gates above the quantum well stack; wherein the plurality of first gates are arranged in electrically continuous rows extending in a first direction, and the plurality of second gates are arranged in electrically continuous rows extending in a second direction perpendicular to the first direction.



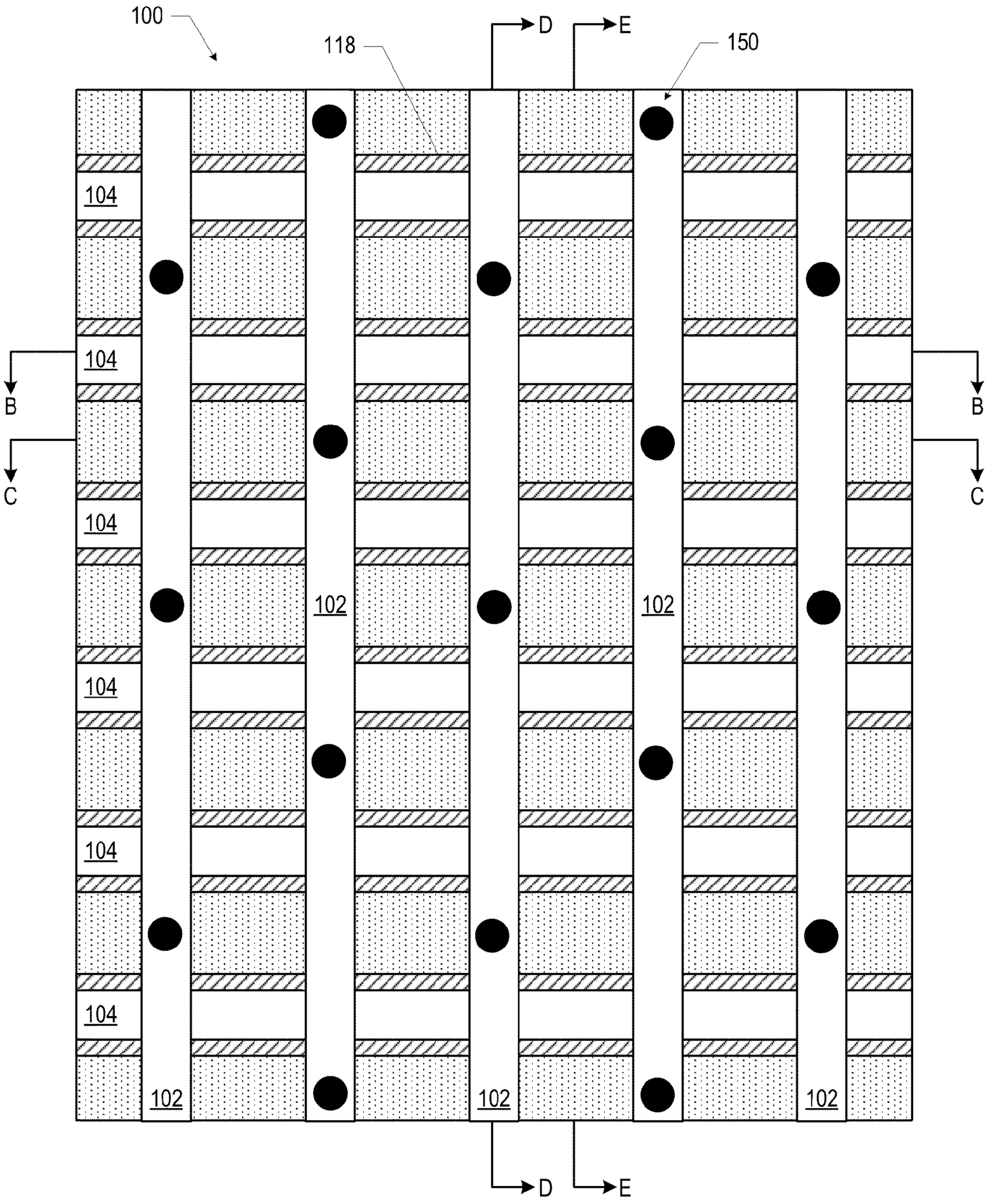

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FIG. 1A

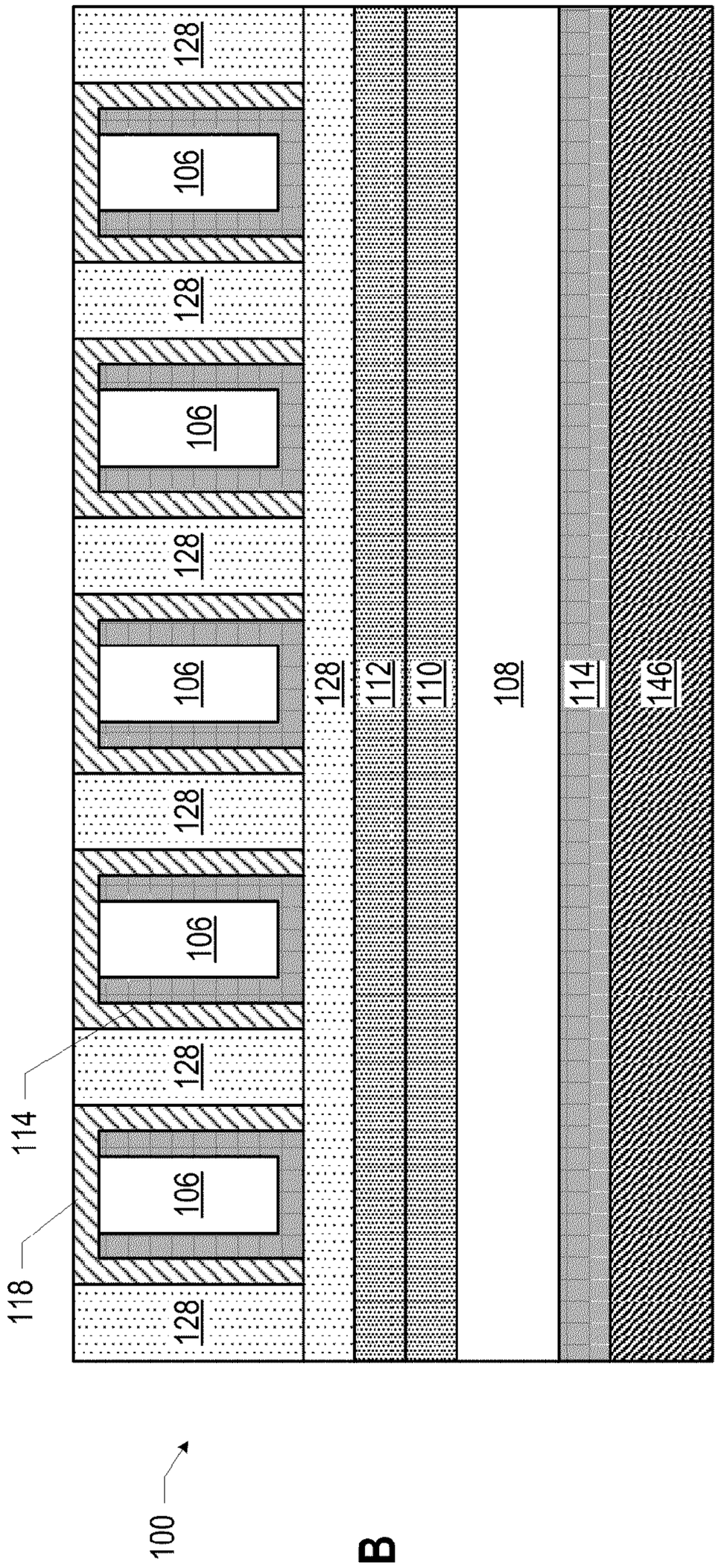
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FIG. 1B

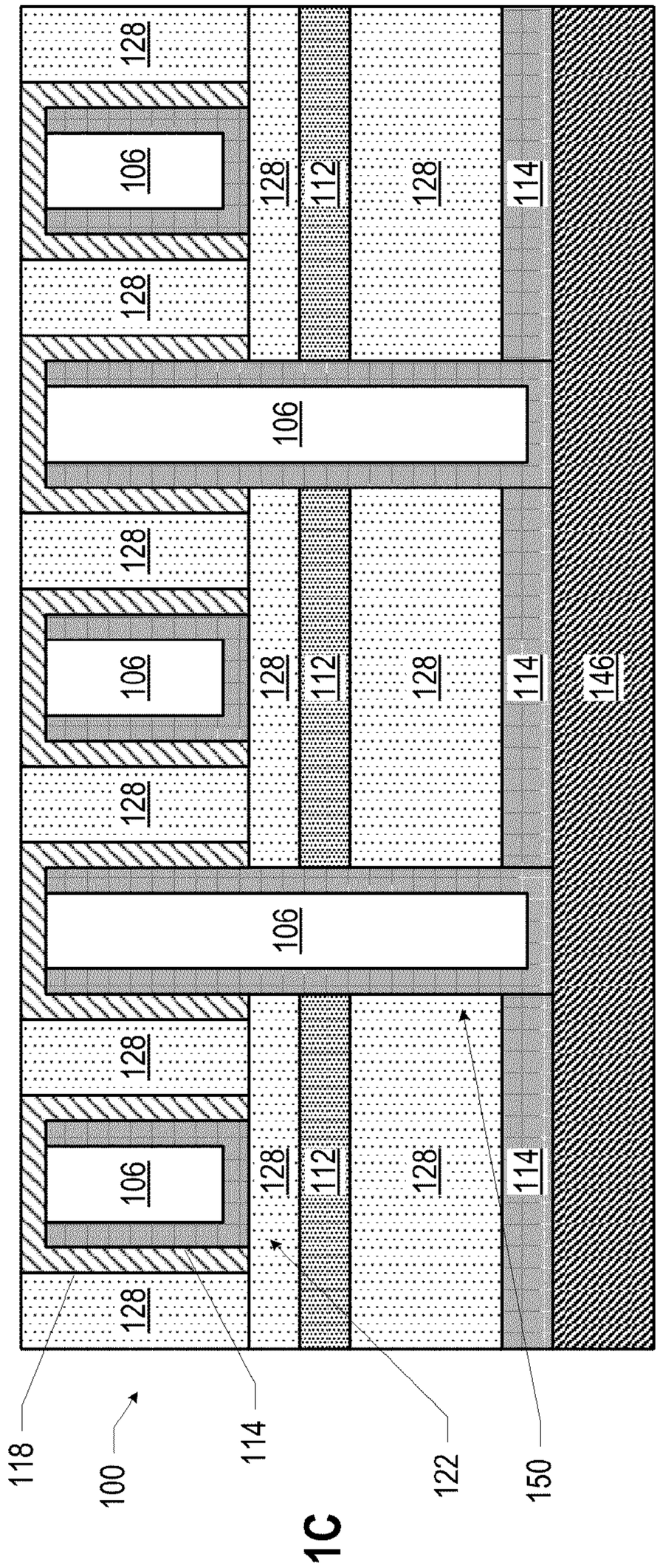
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FIG. 1C

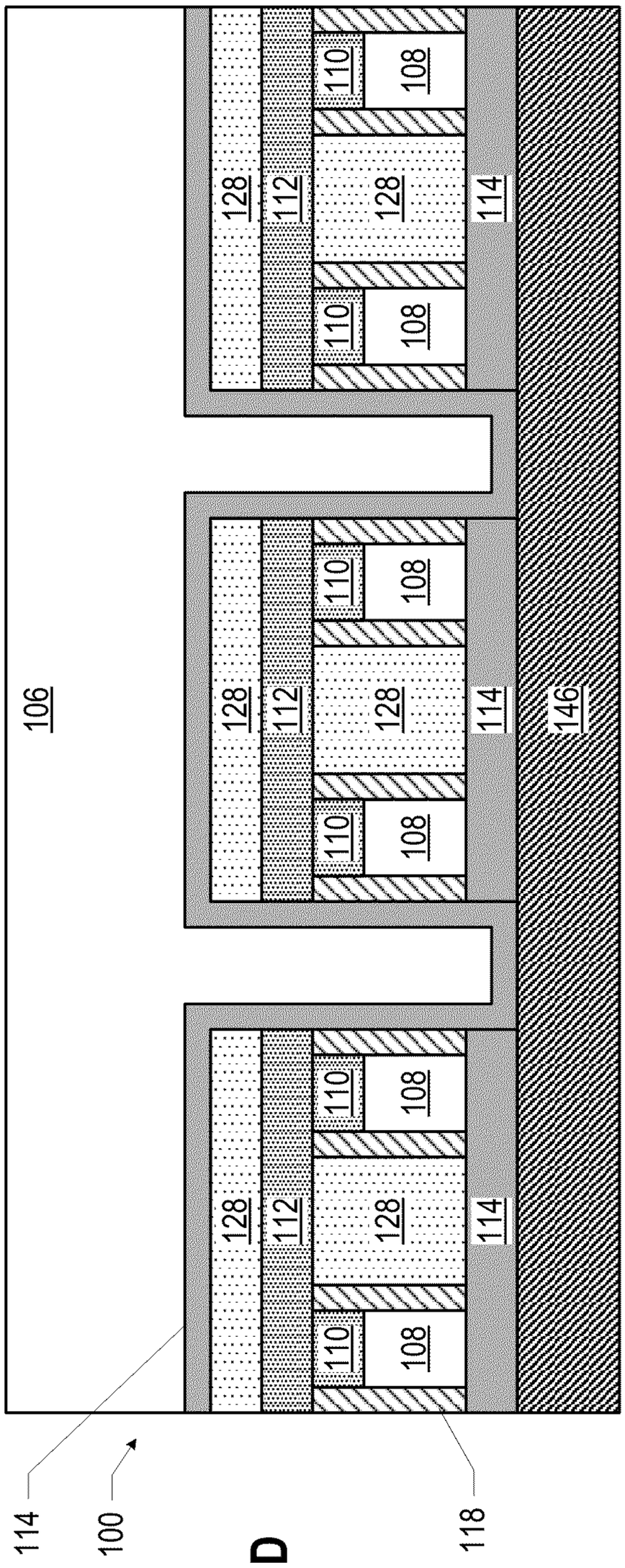
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FIG. 1D

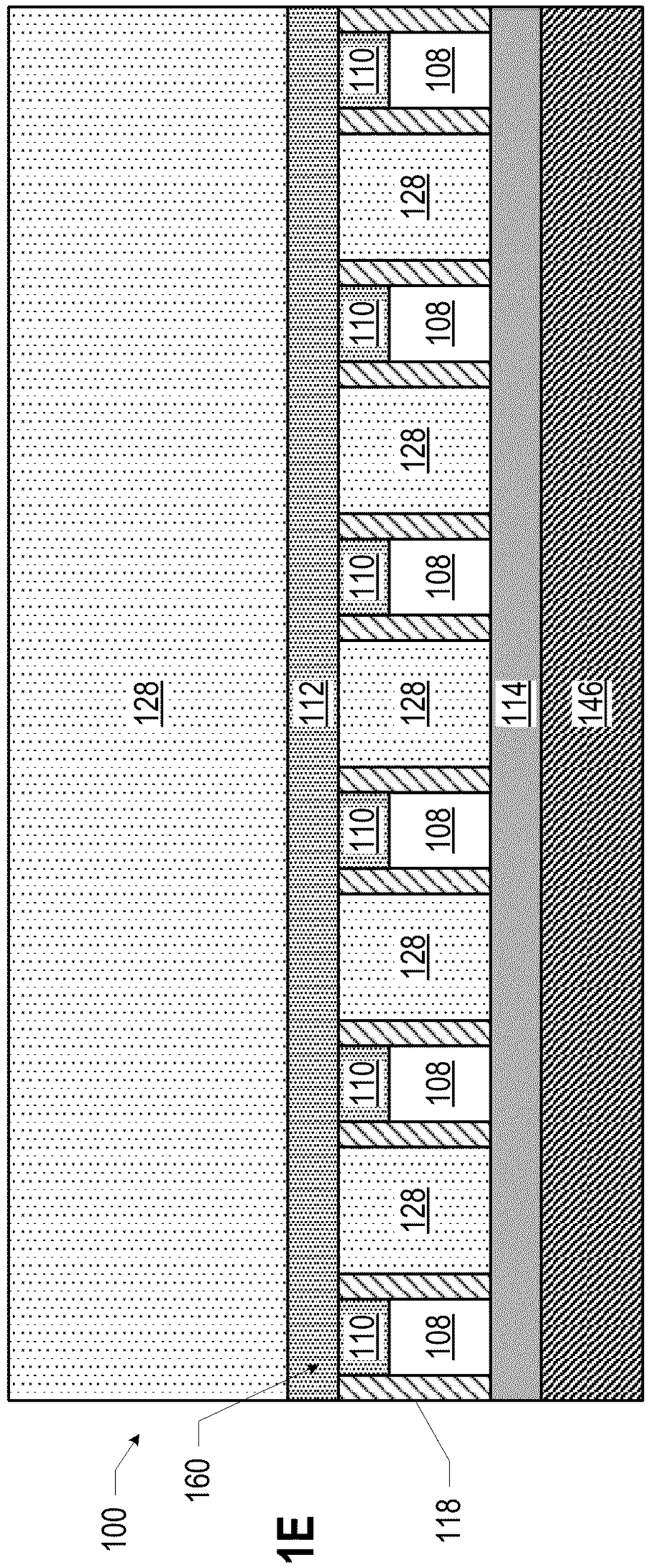
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FIG. 1E

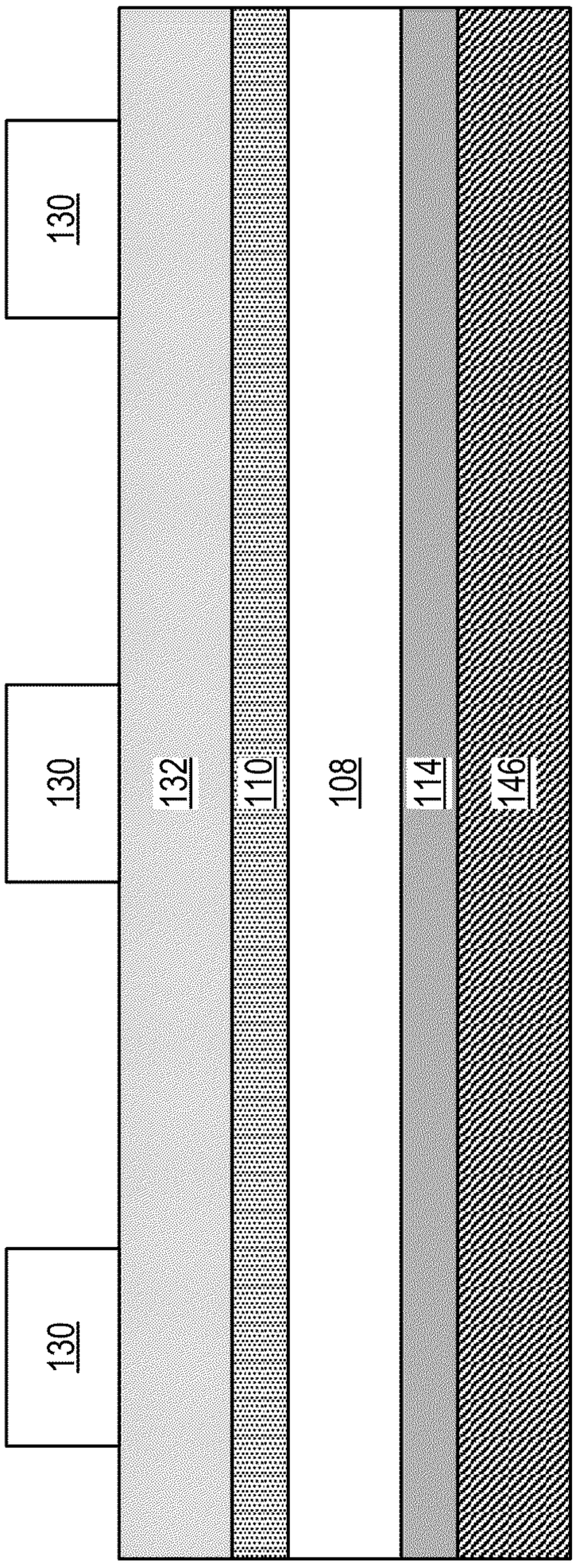

FIG. 2A

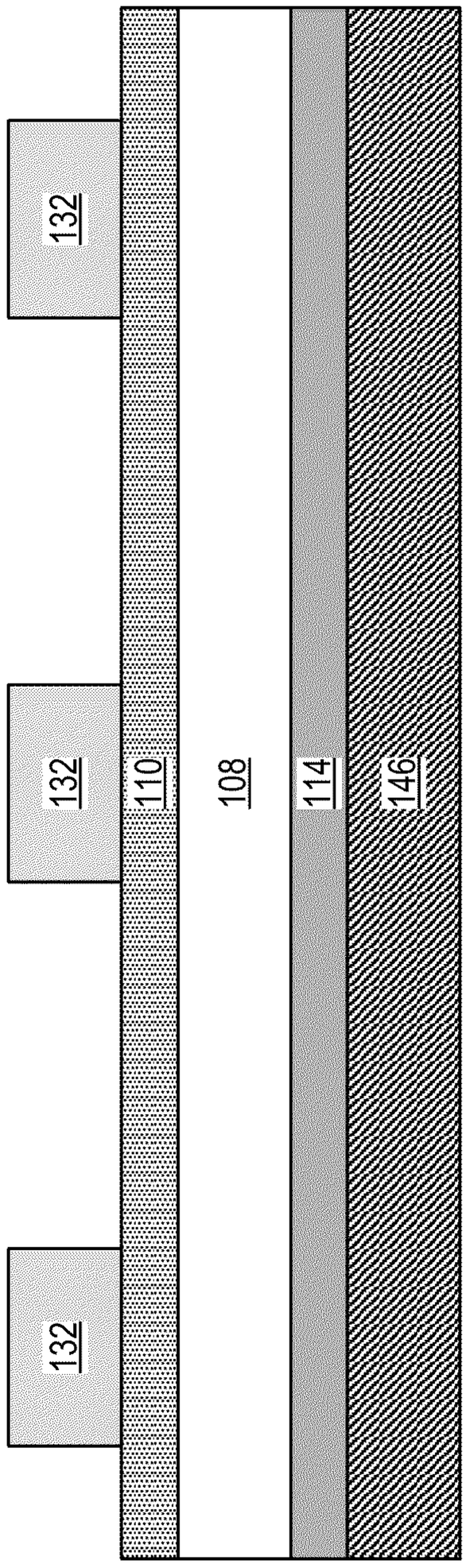

FIG. 2B

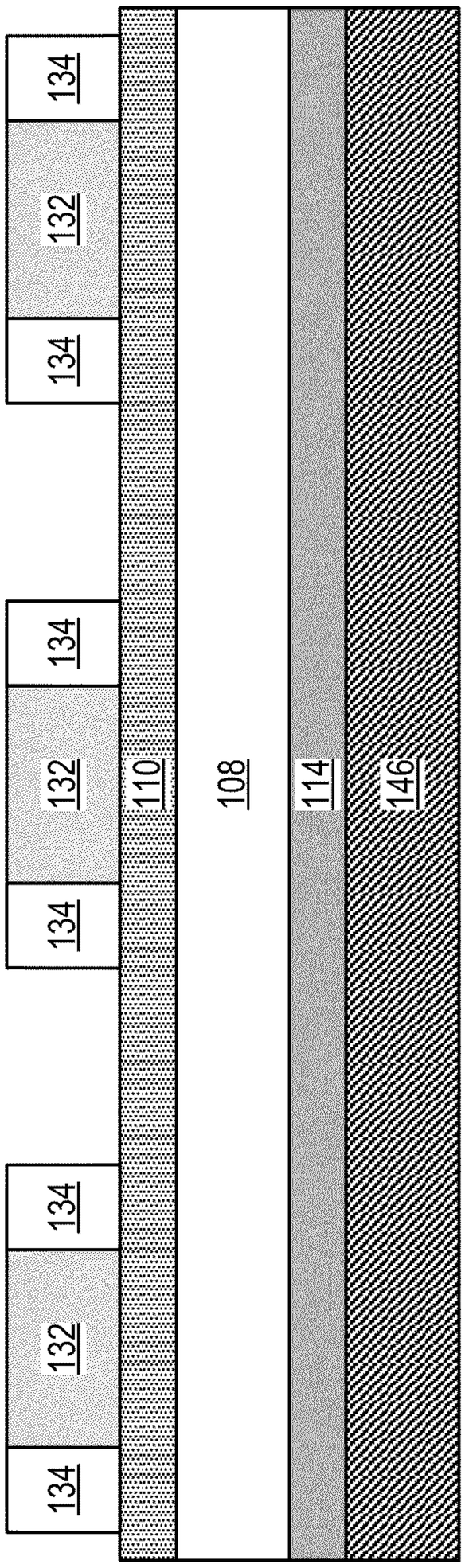
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FIG. 2C

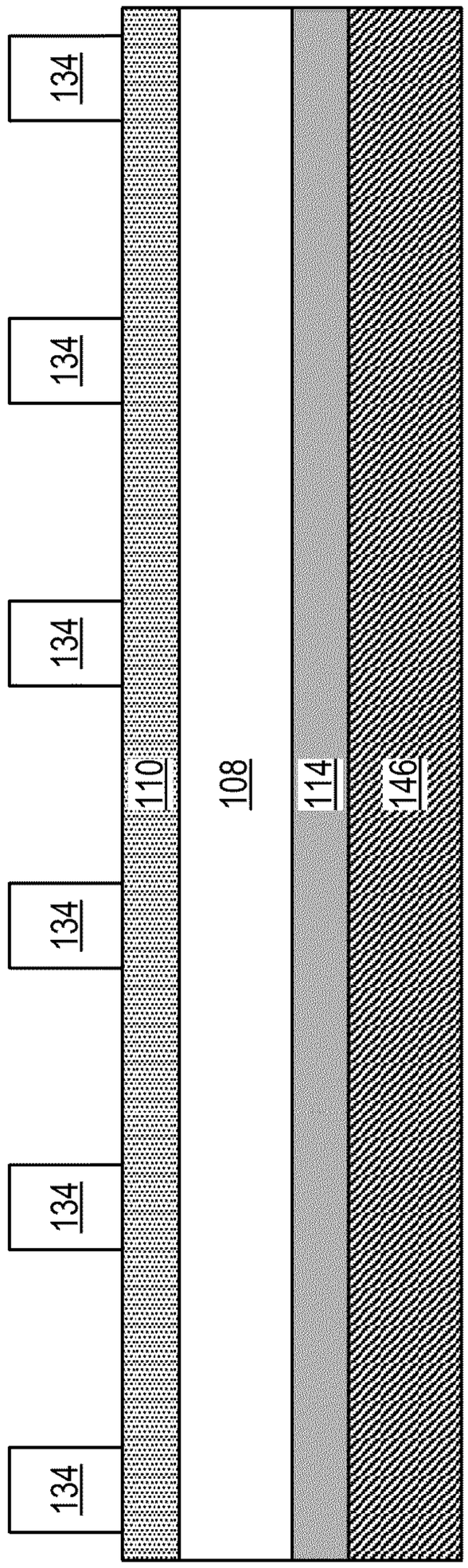
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FIG. 2D

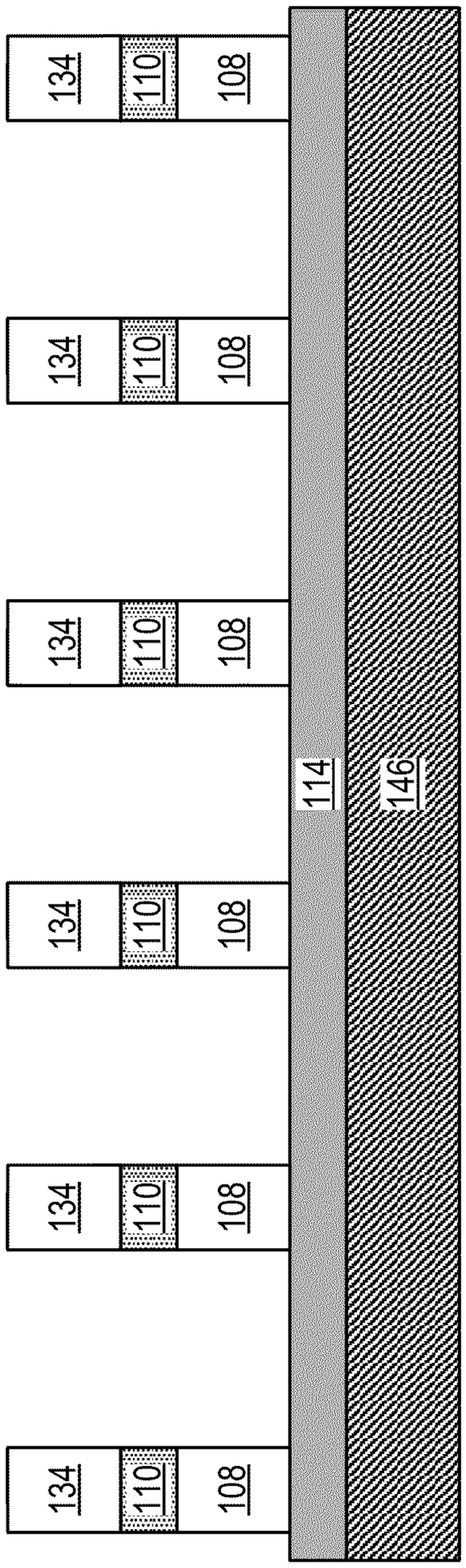

FIG.2E

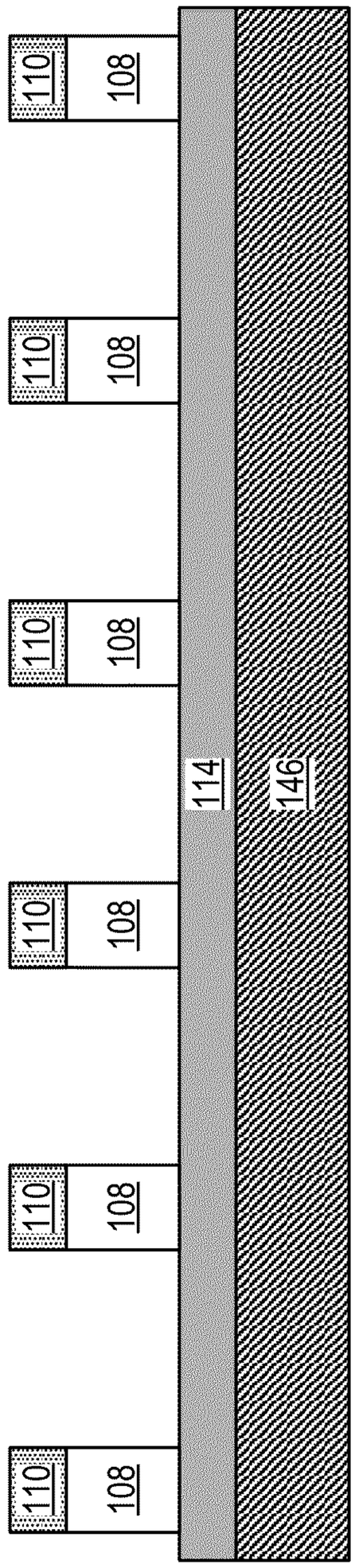

FIG. 2F

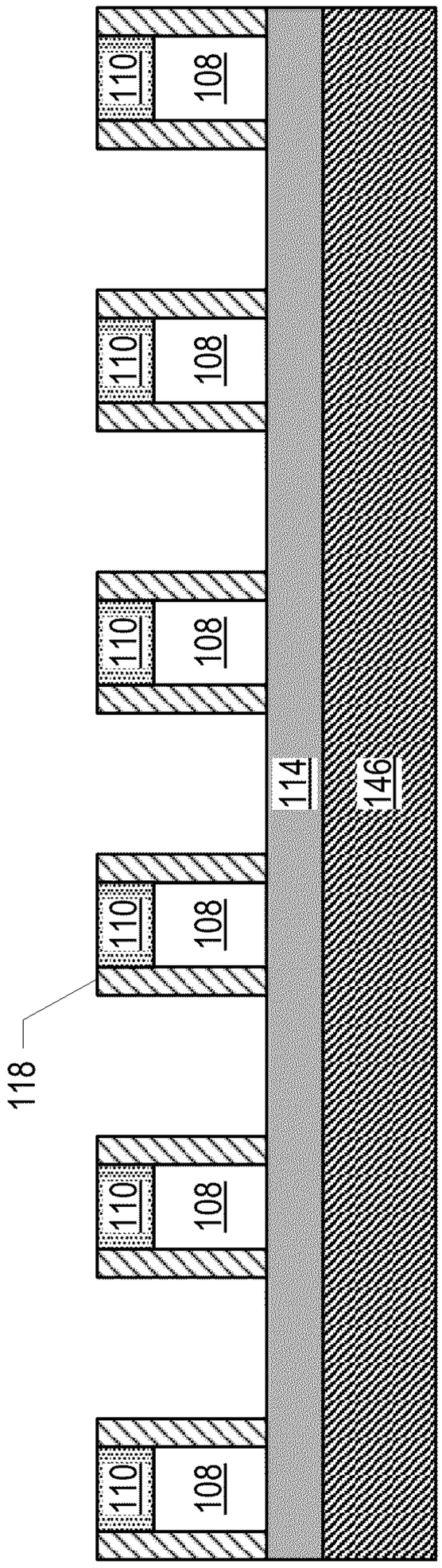

FIG. 2G

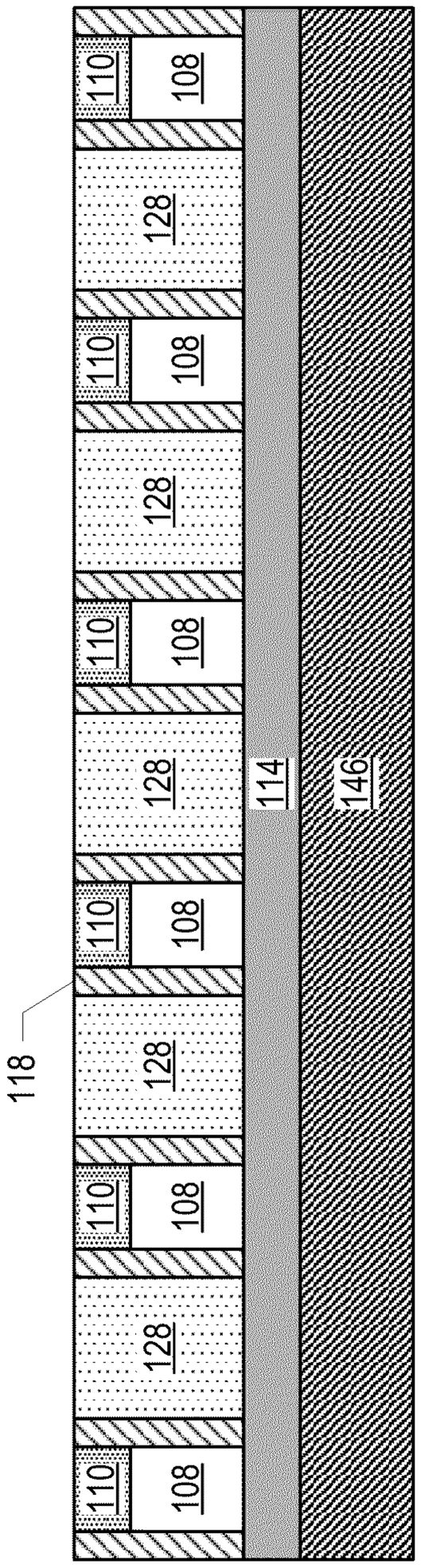

FIG. 2H

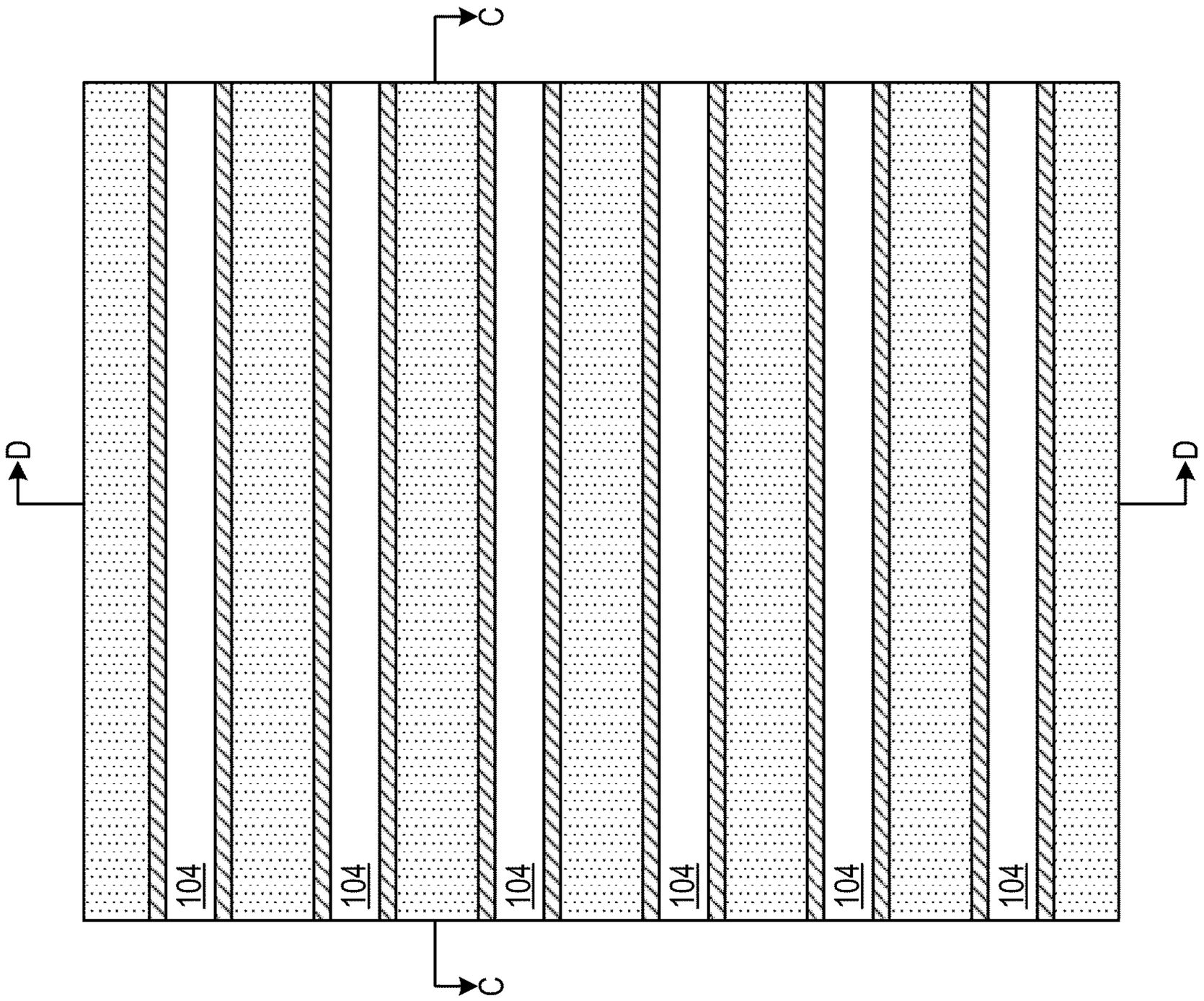

FIG. 2I

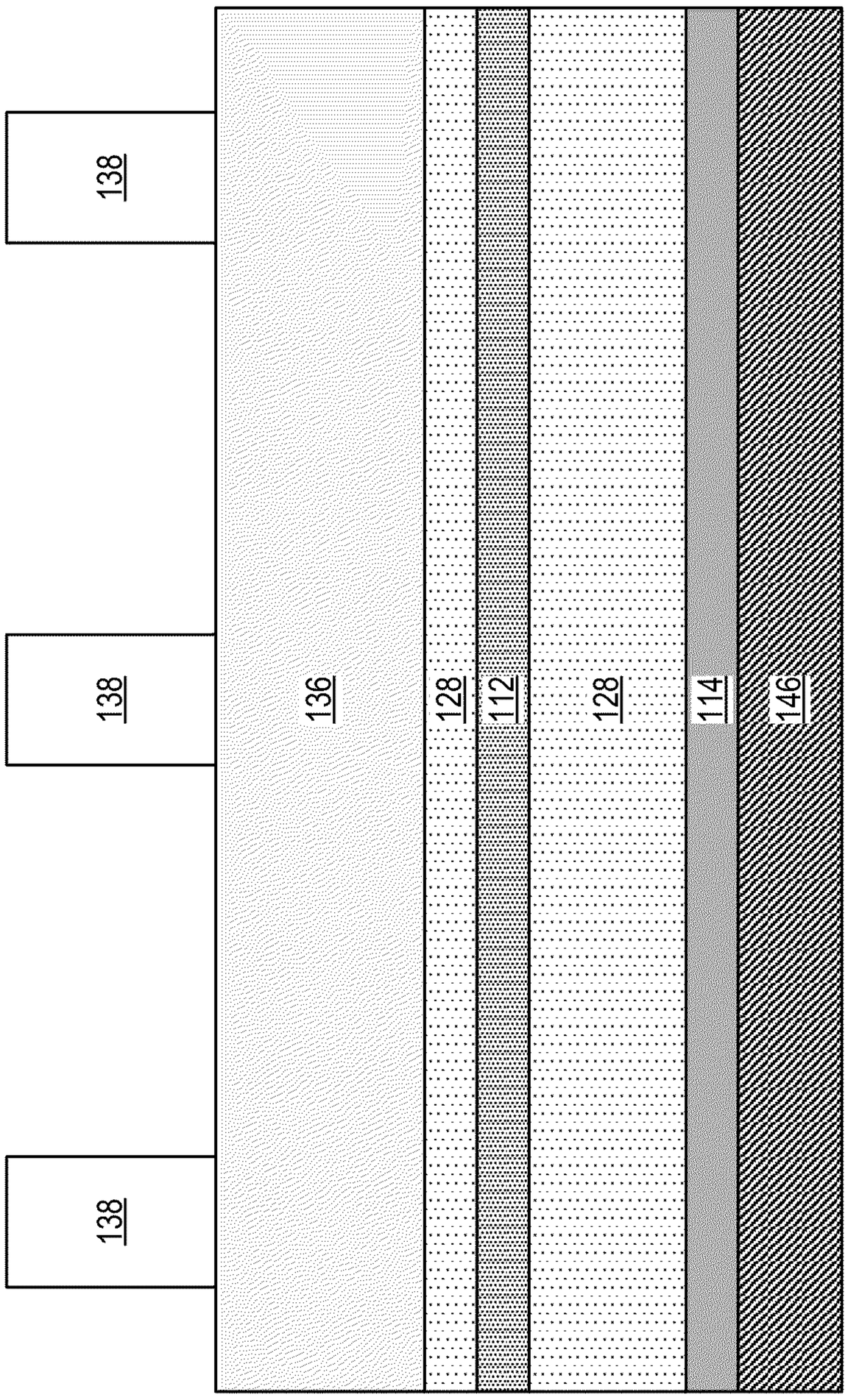

FIG. 2J

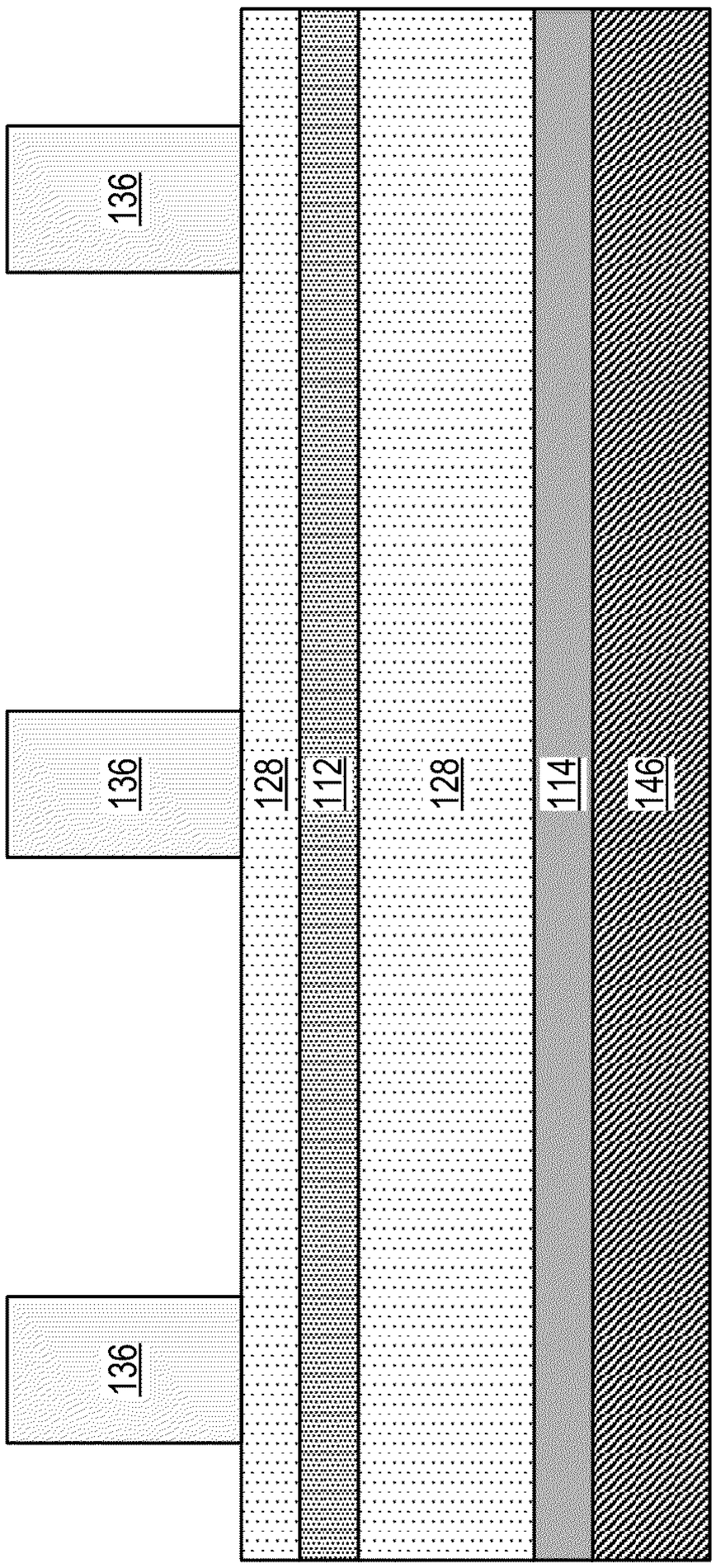

FIG. 2K

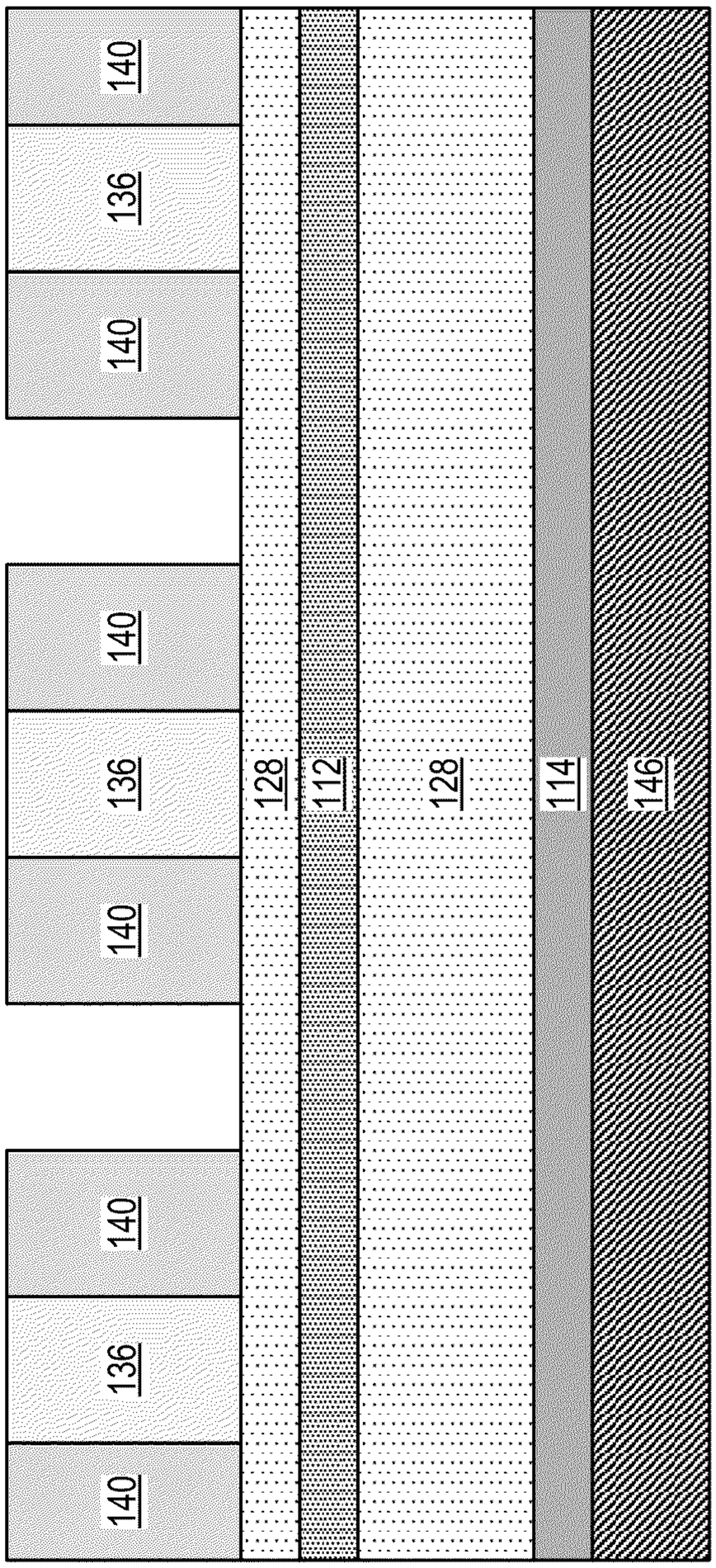

FIG. 2L

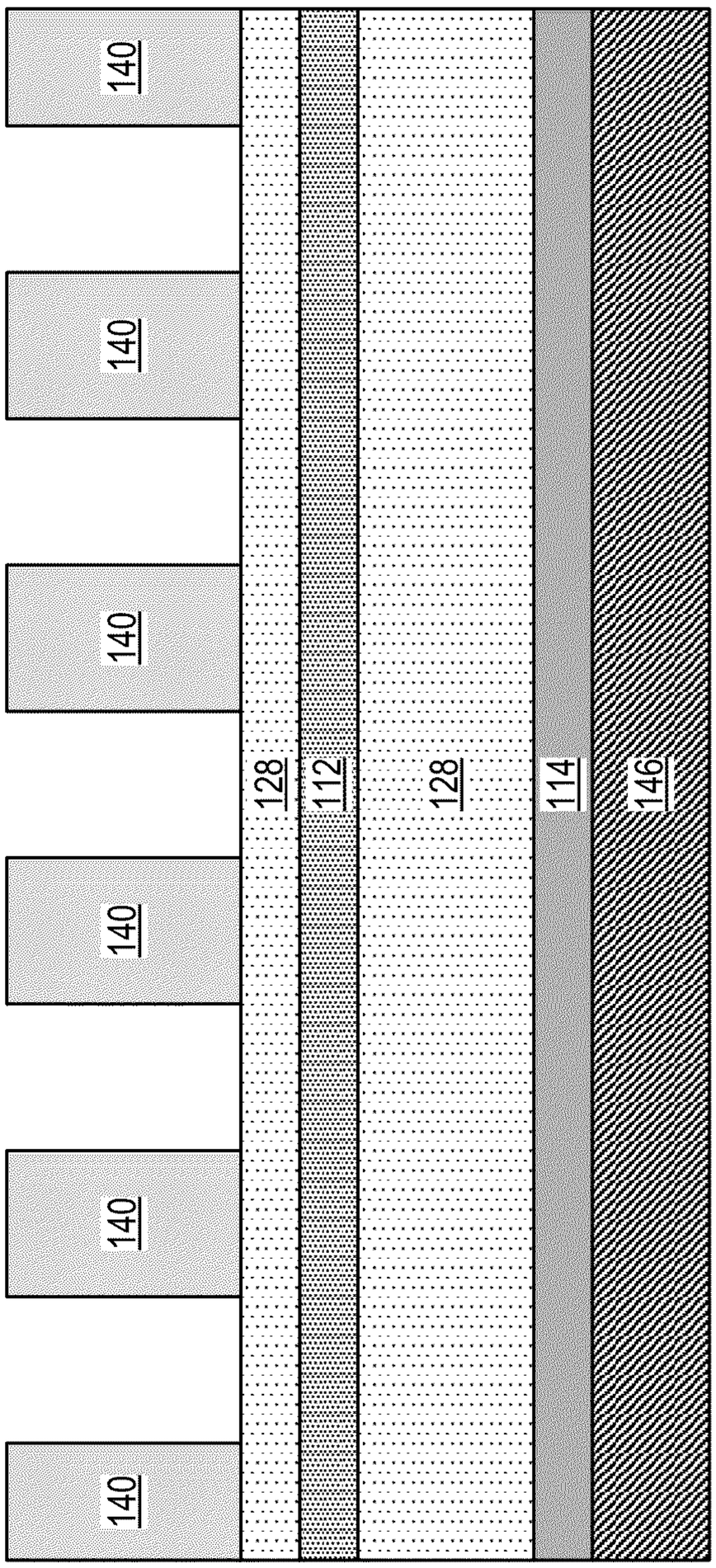

FIG. 2M

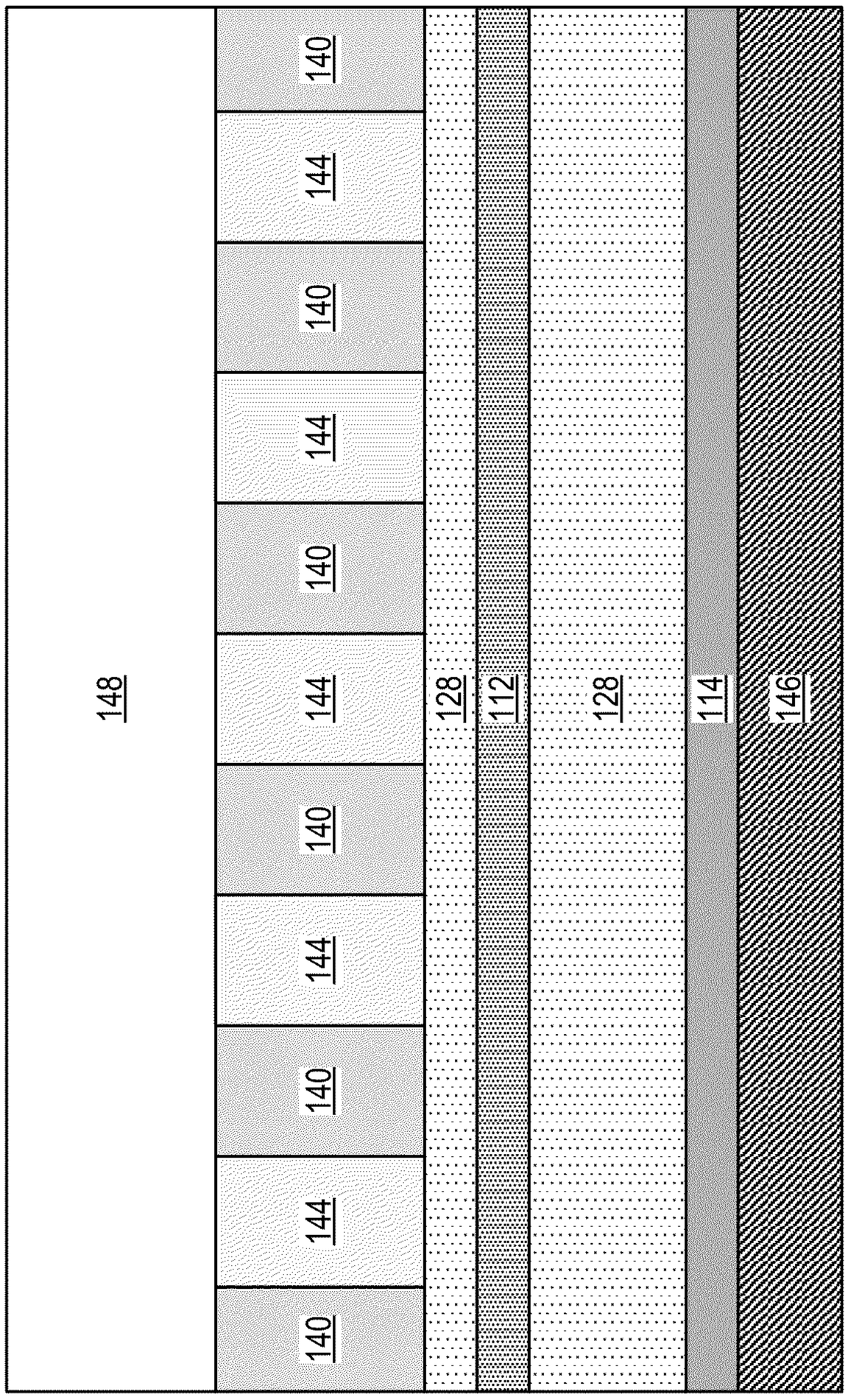

FIG. 2N

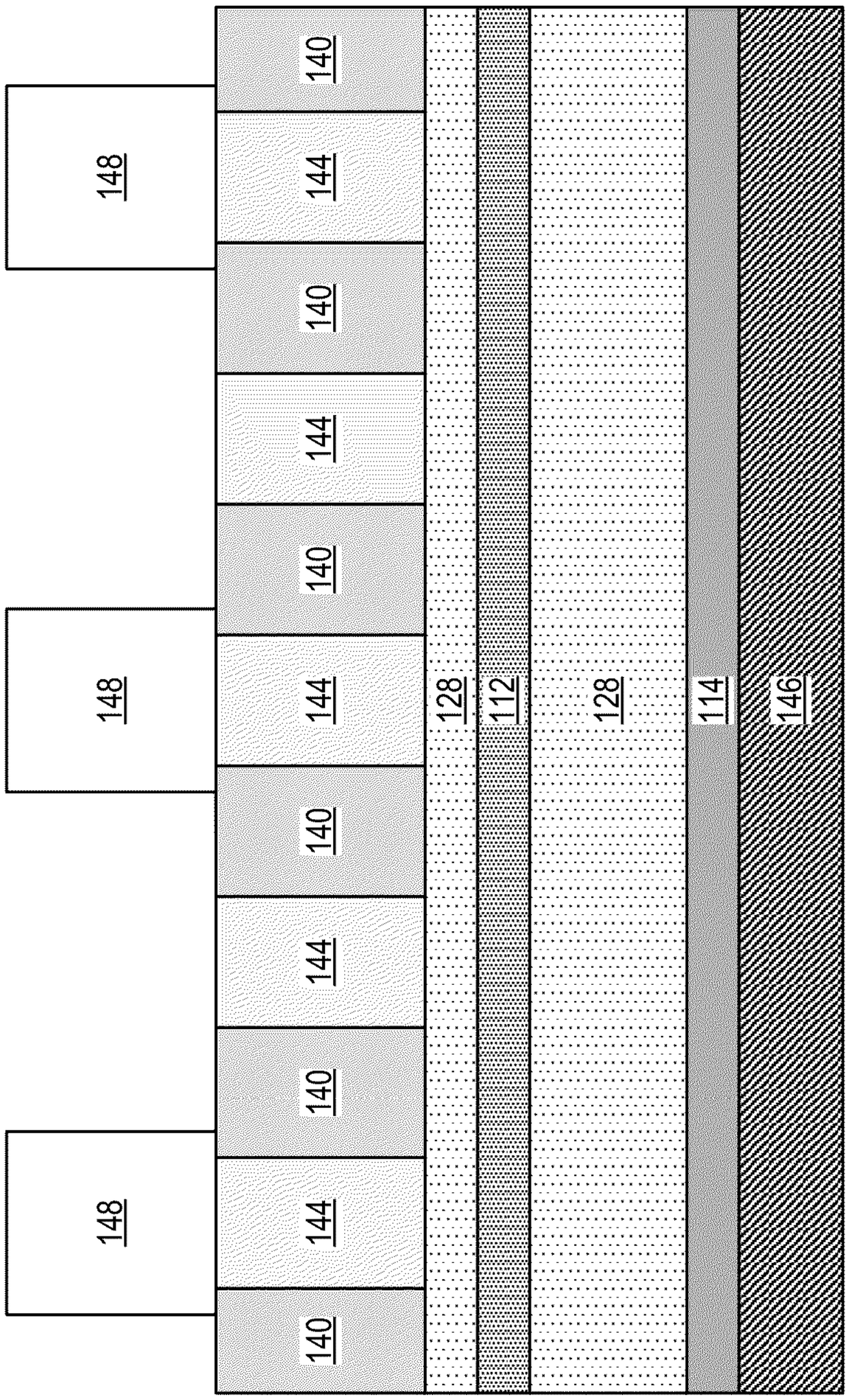
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FIG. 2O

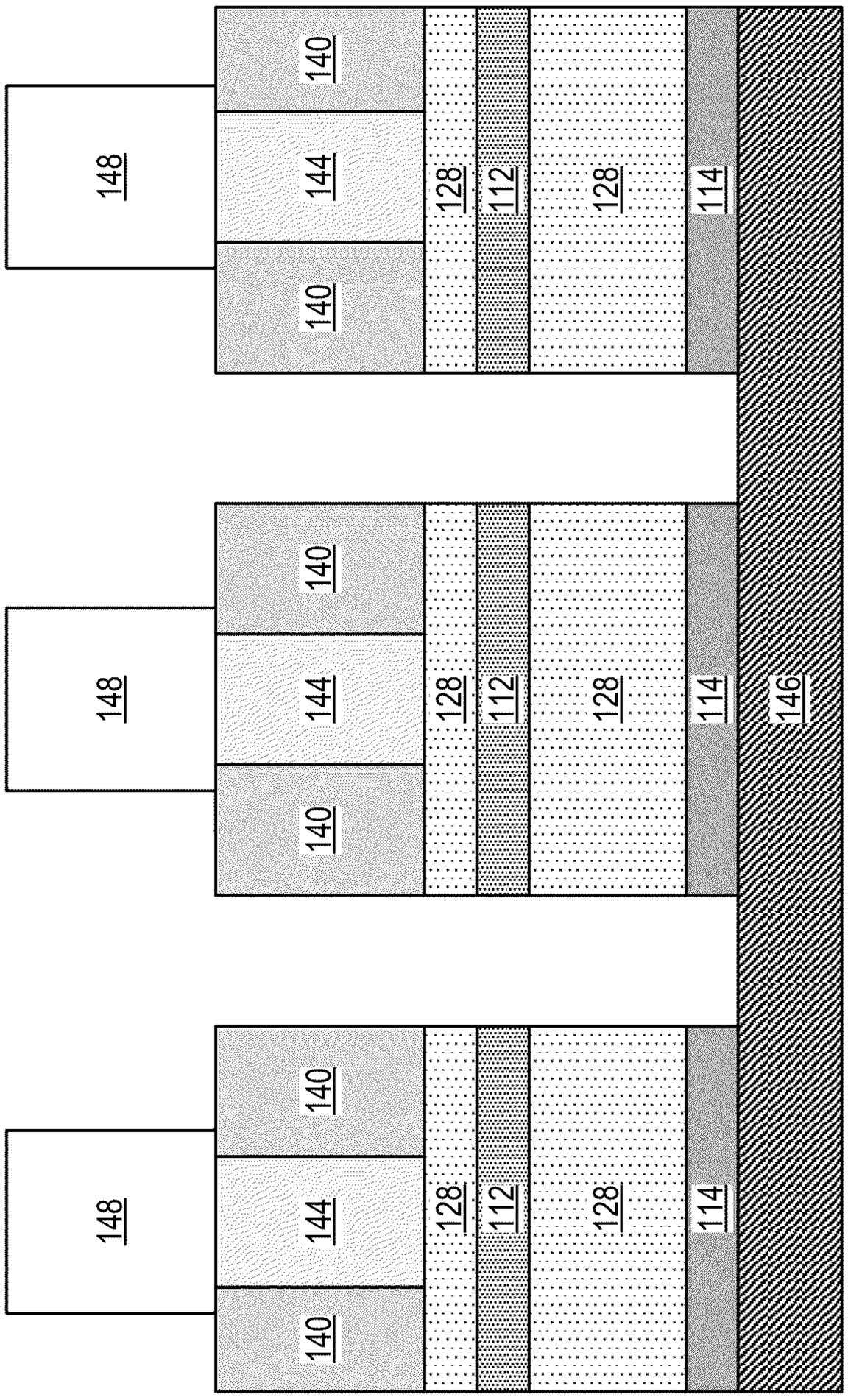

FIG. 2P

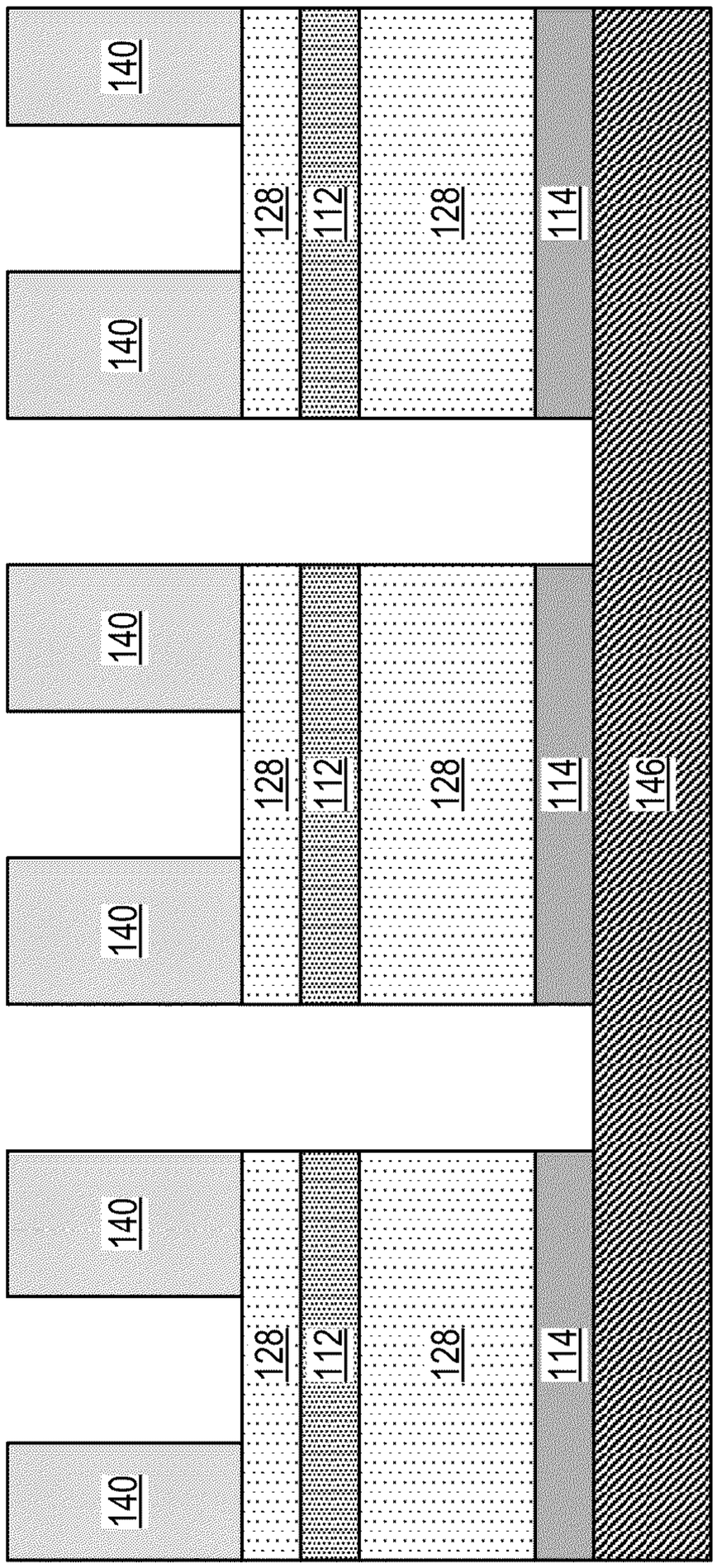
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FIG. 2Q

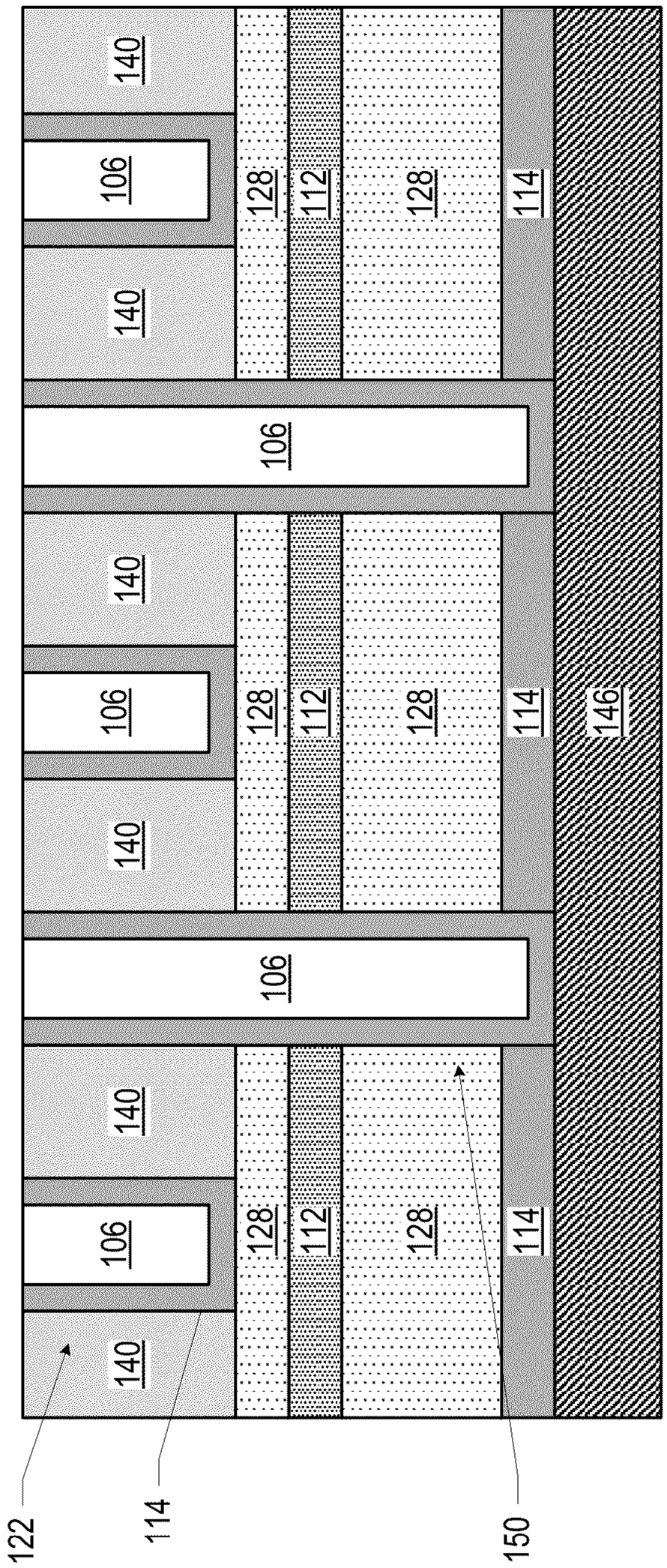
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FIG. 2R

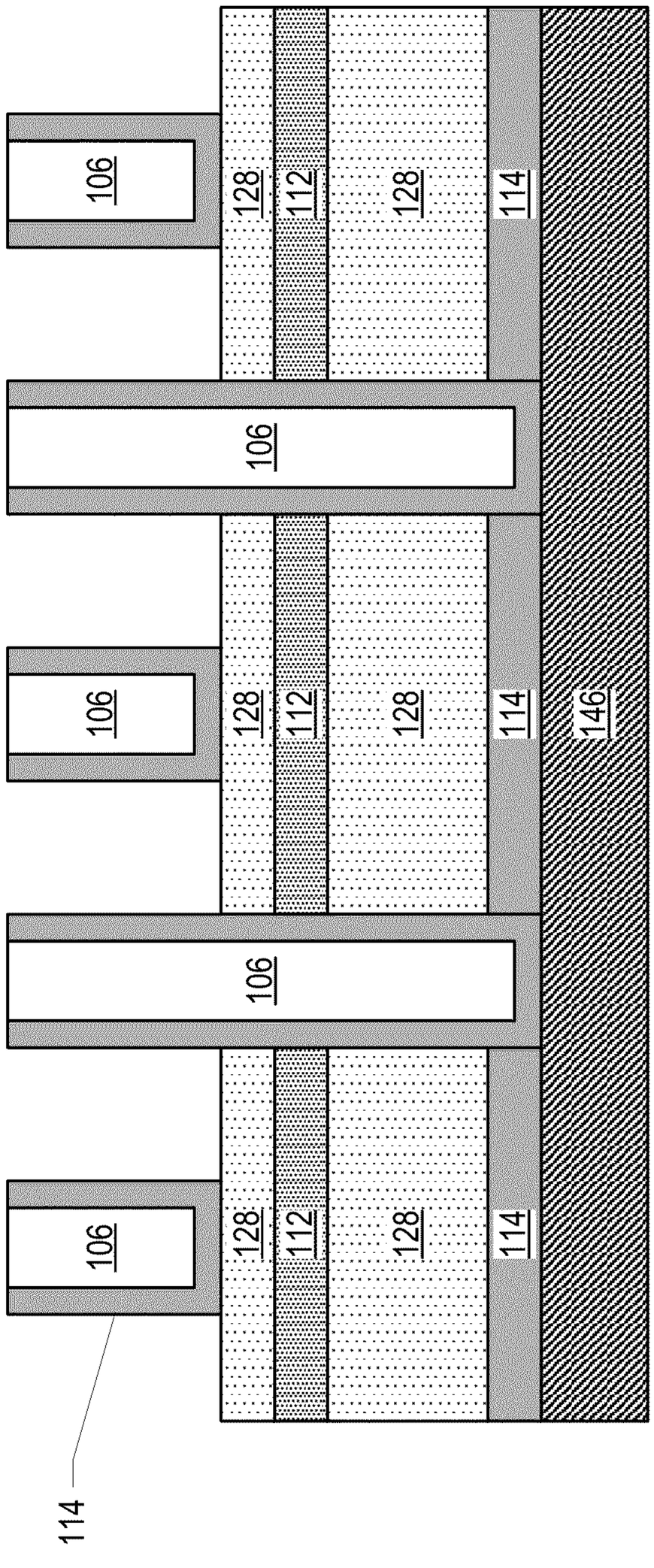
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FIG. 2S

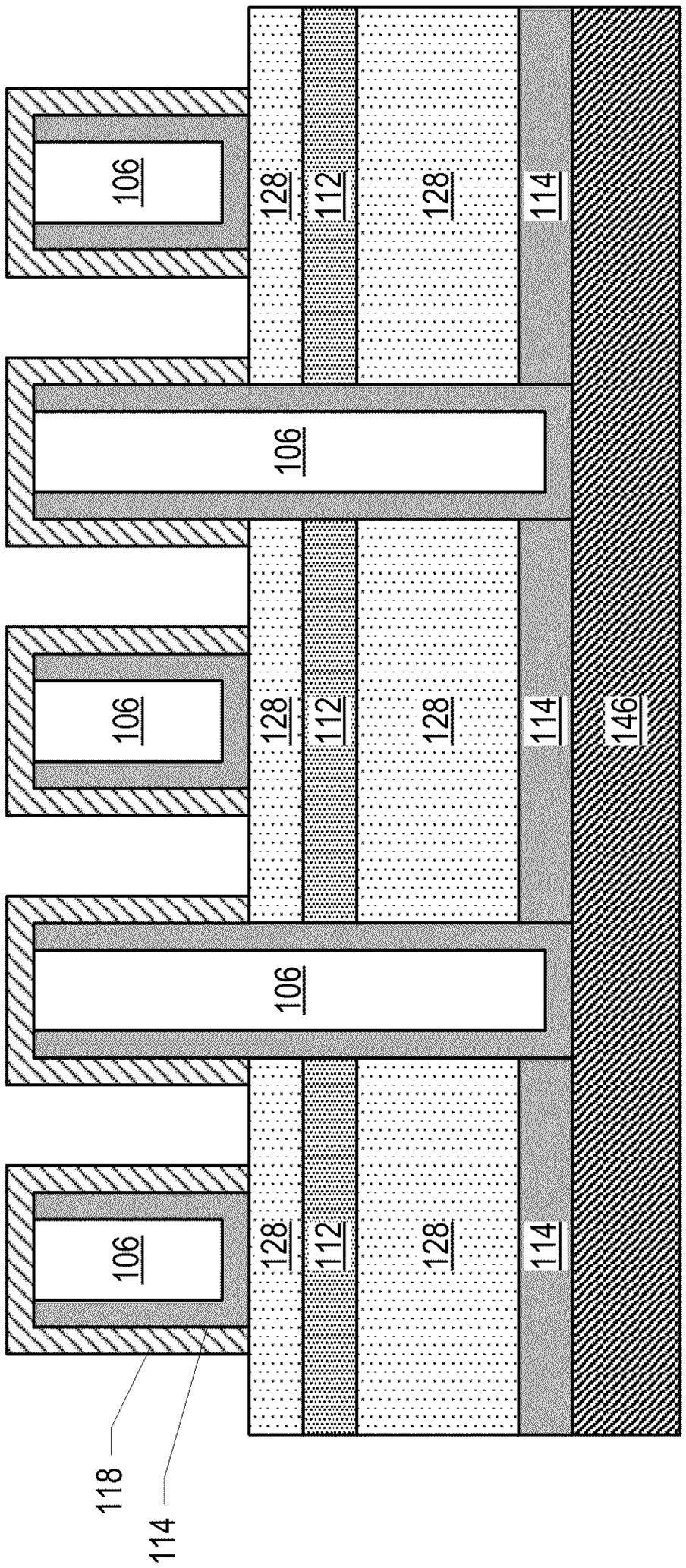
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FIG. 2T

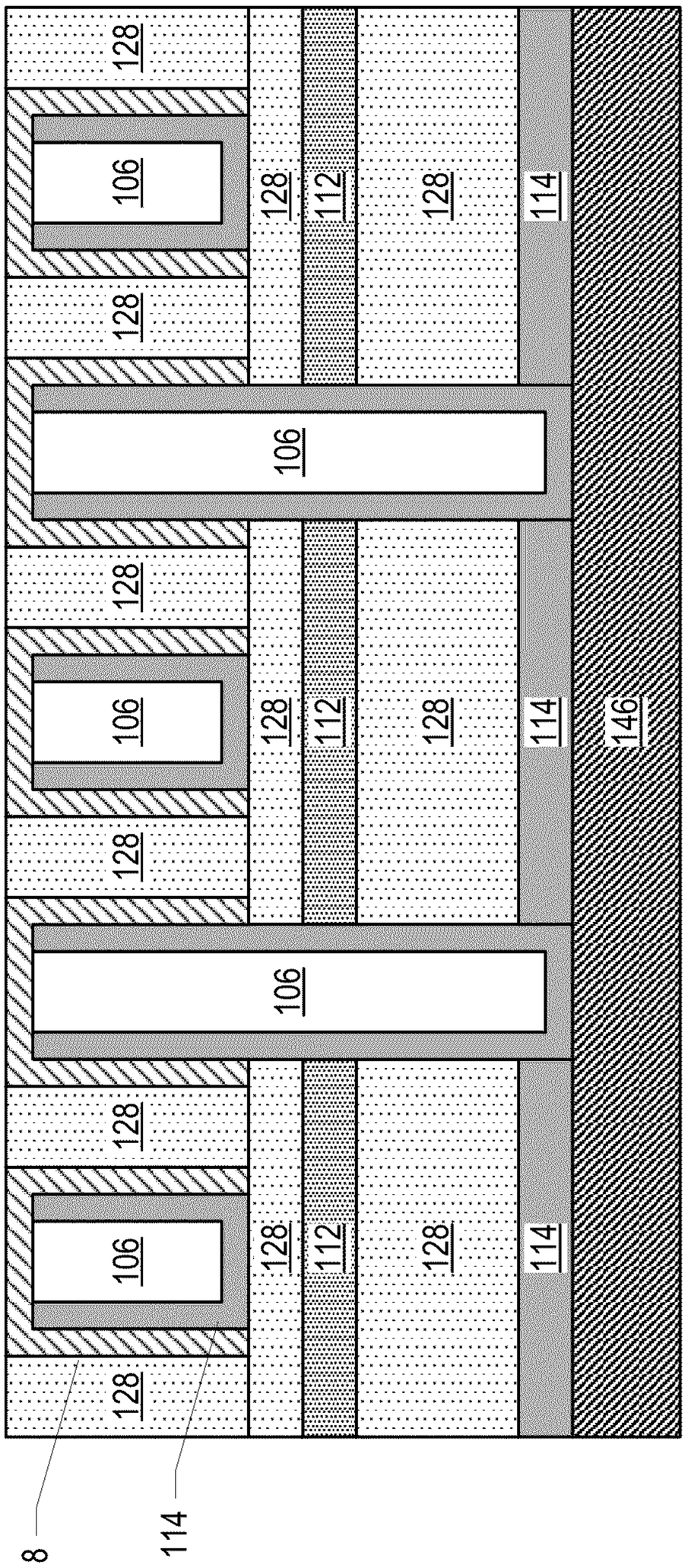
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FIG. 2U

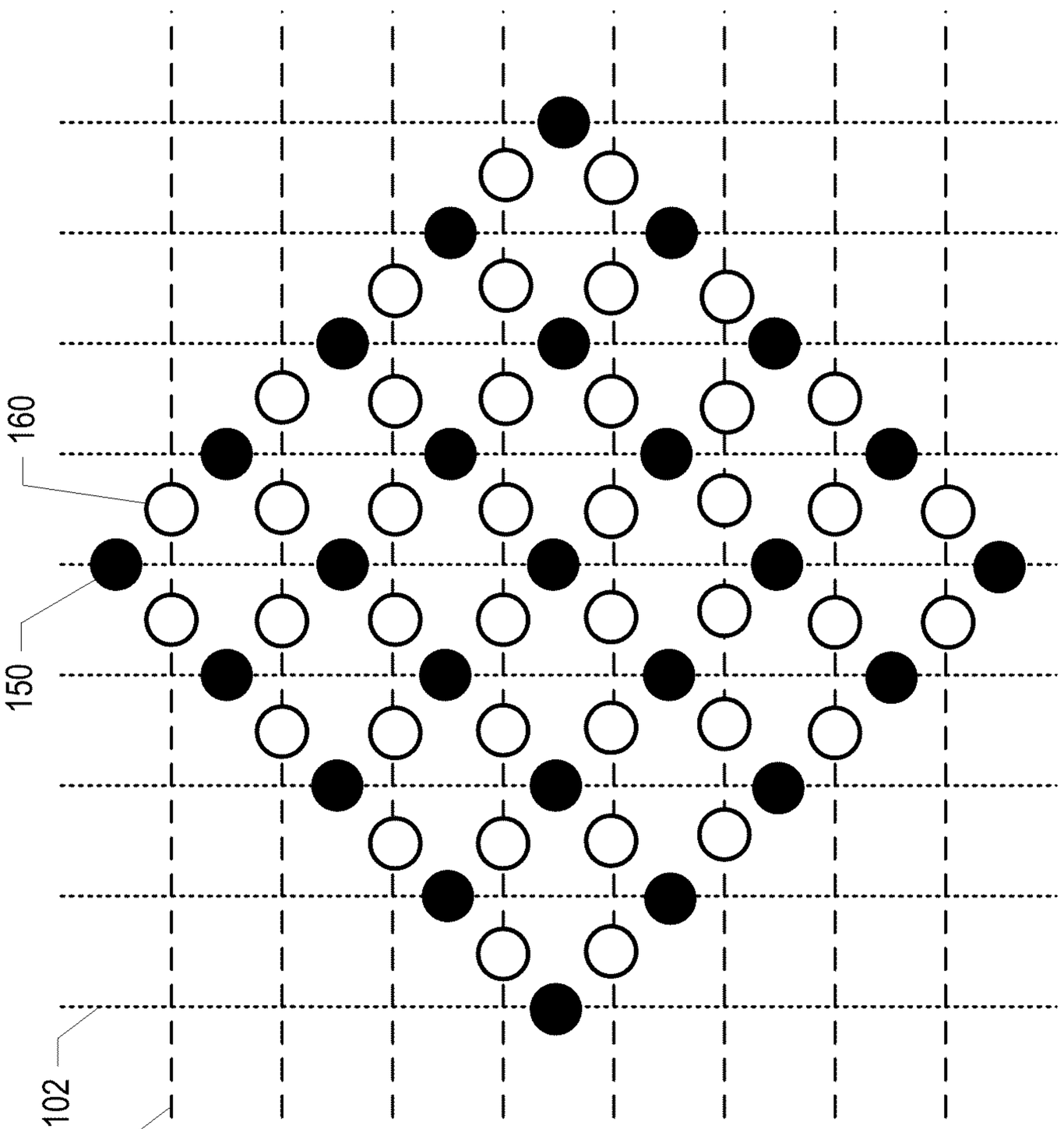


FIG. 3

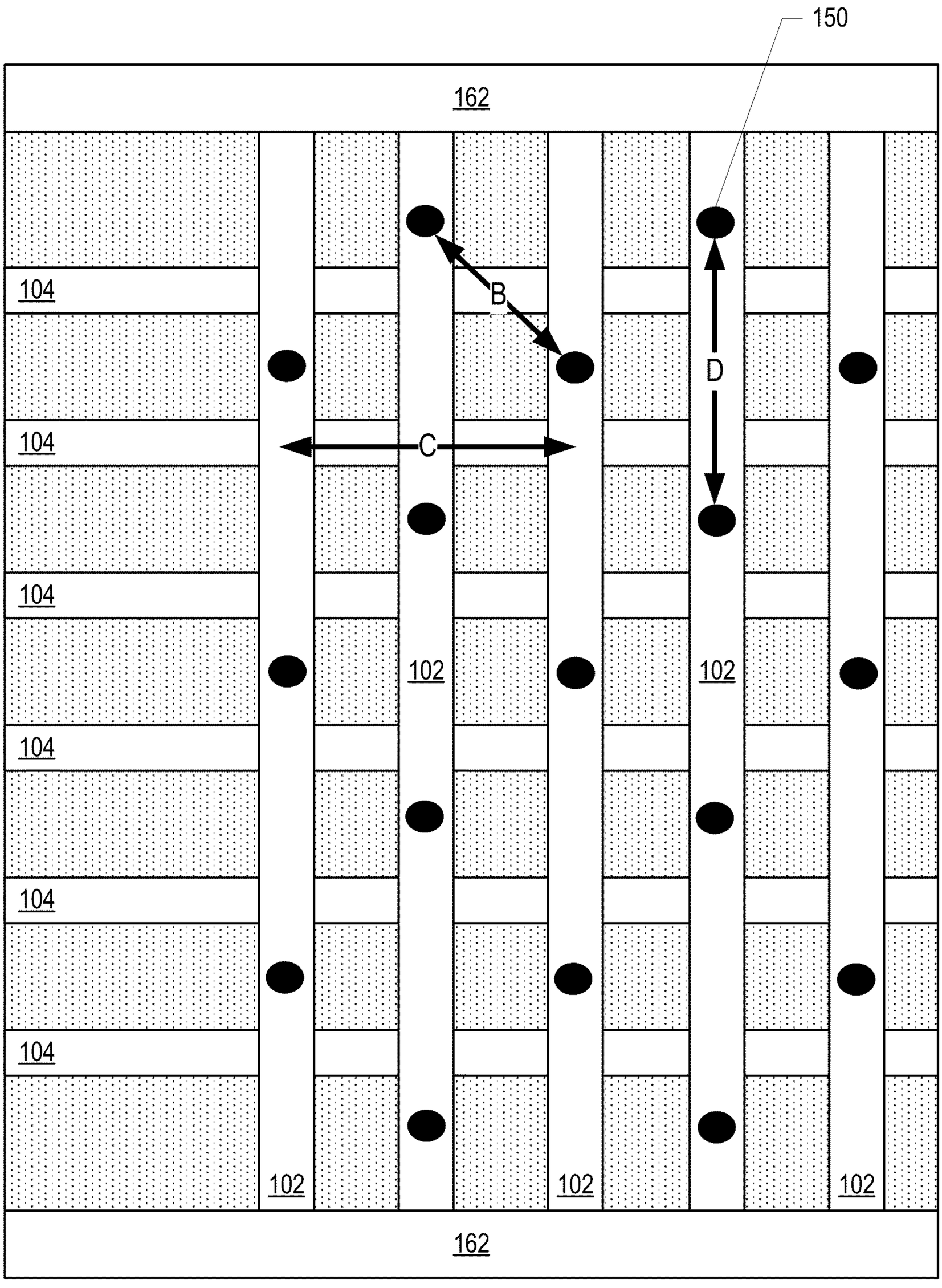


FIG. 4A

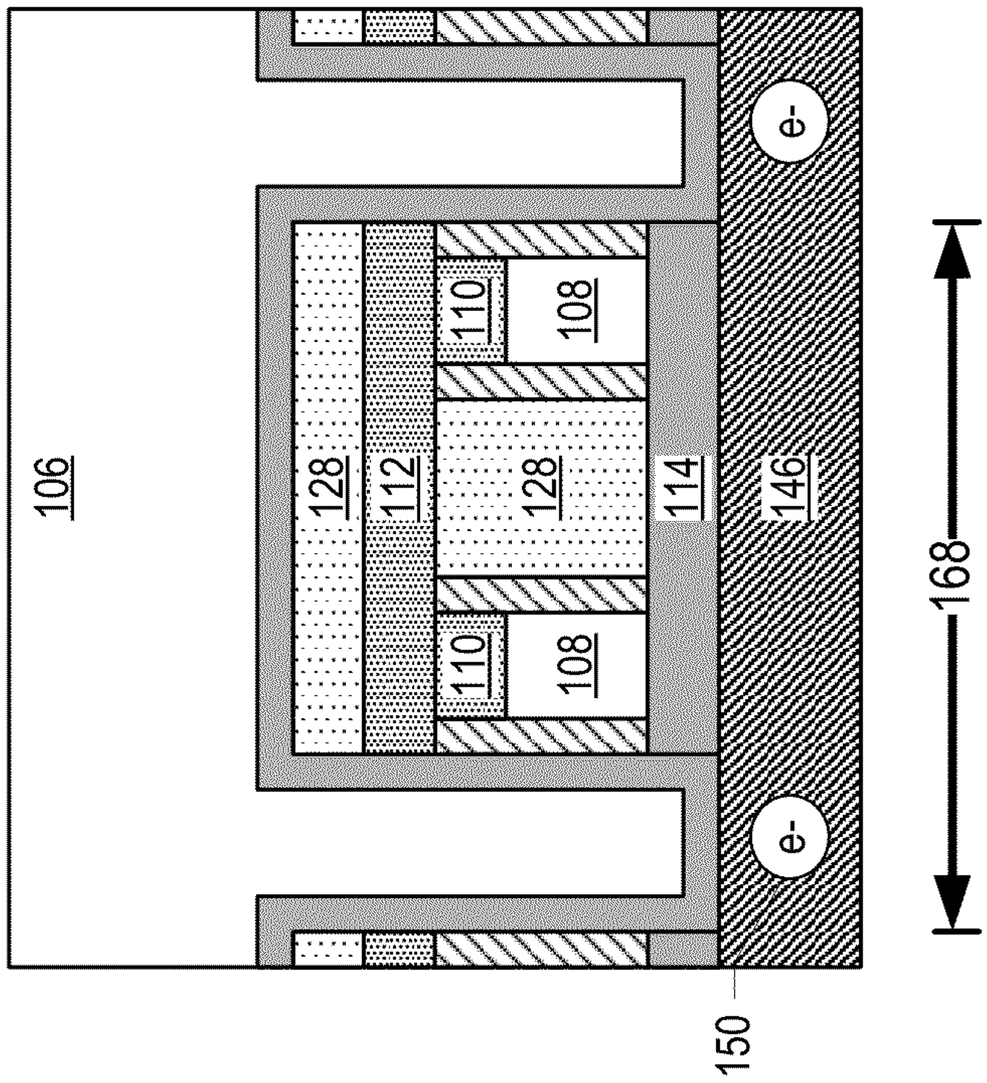


FIG. 4D

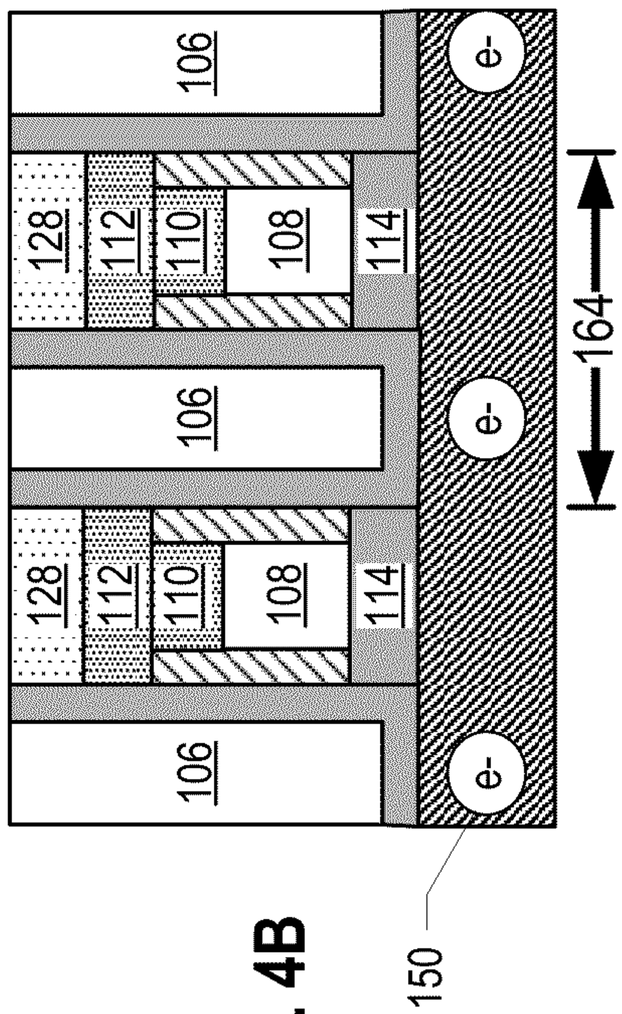


FIG. 4B

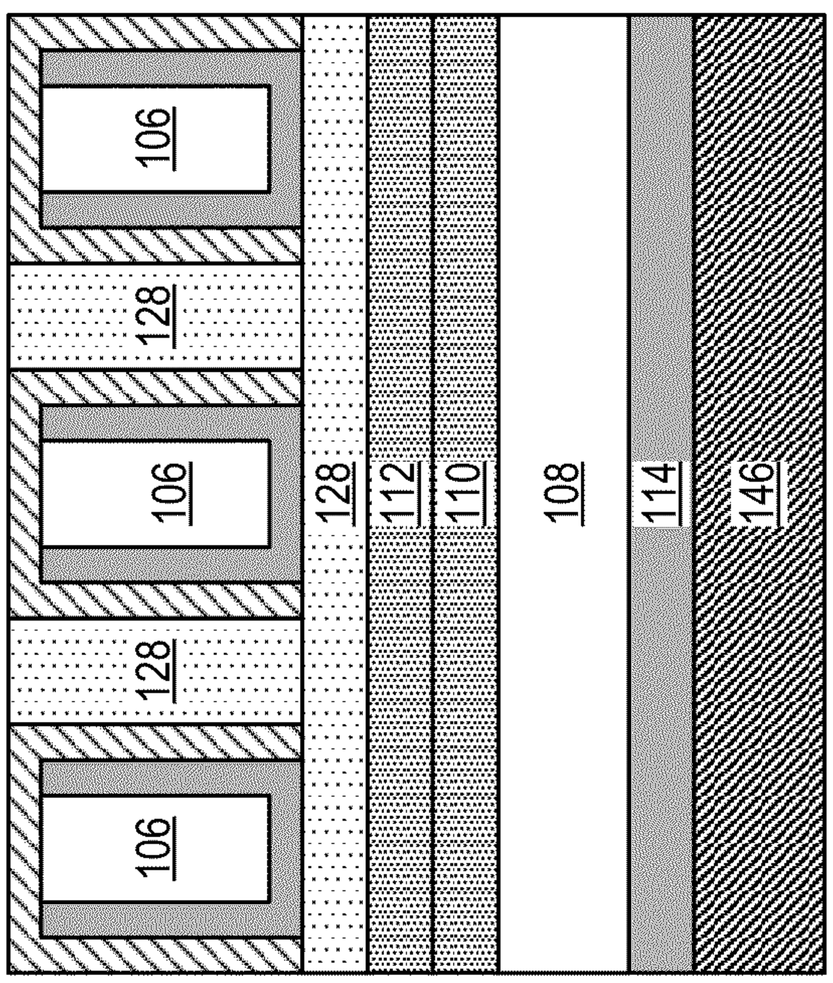


FIG. 4C

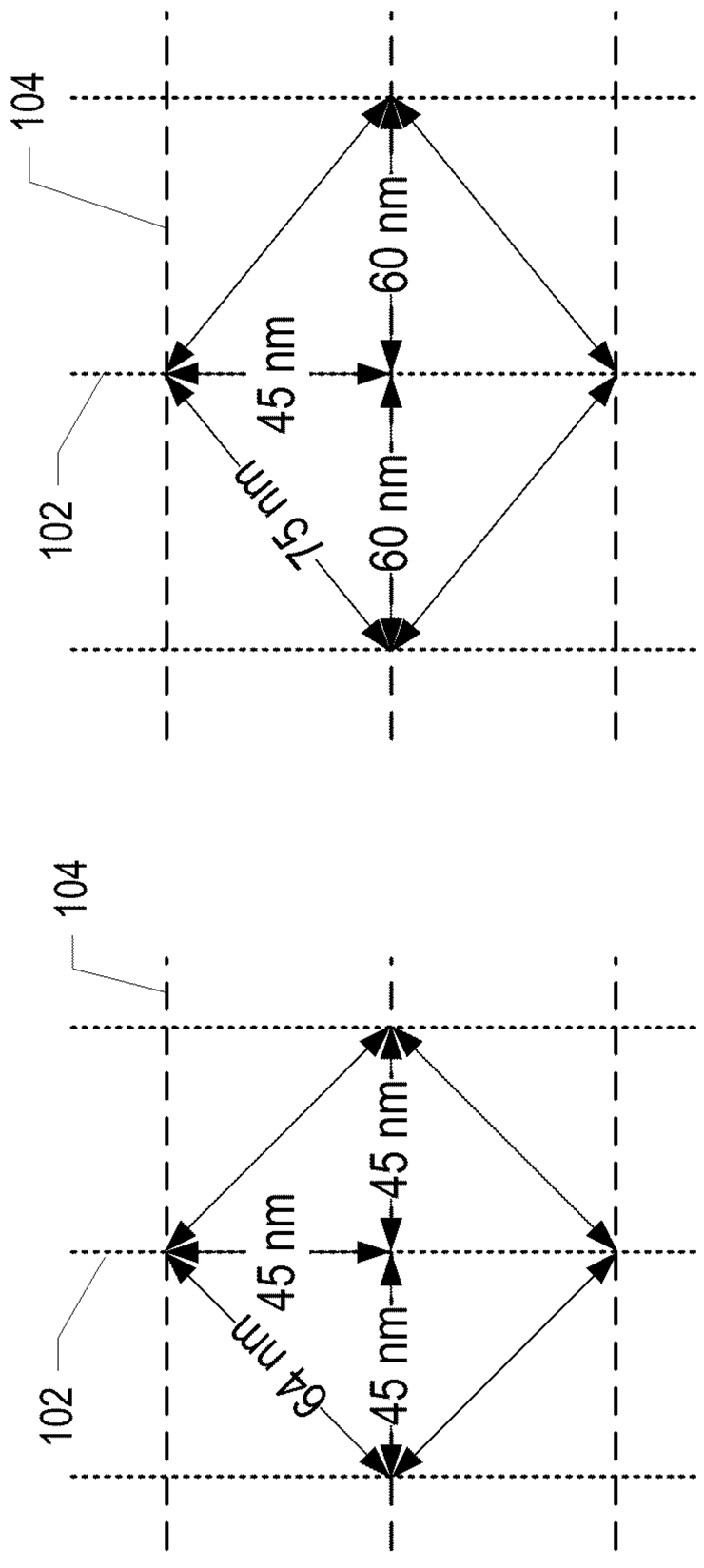


FIG. 5C

FIG. 5B

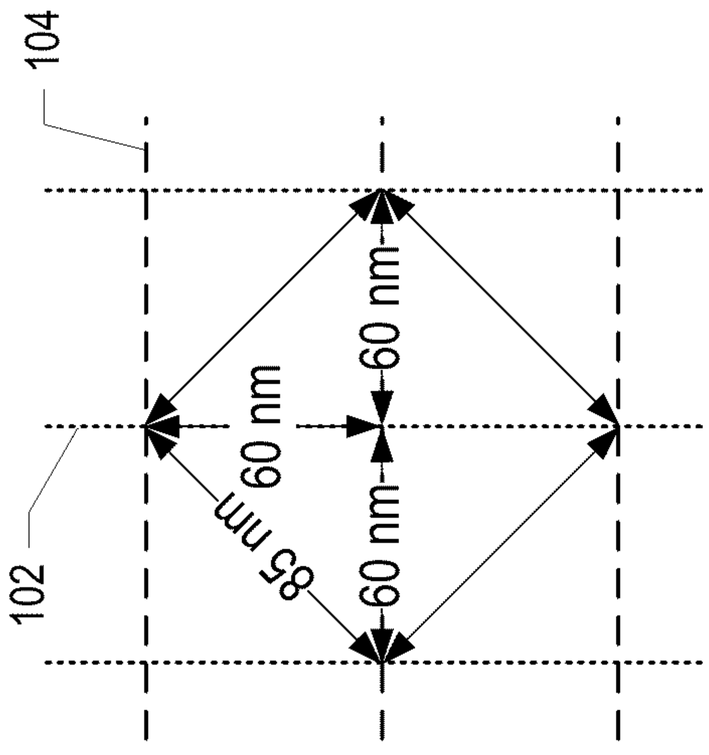
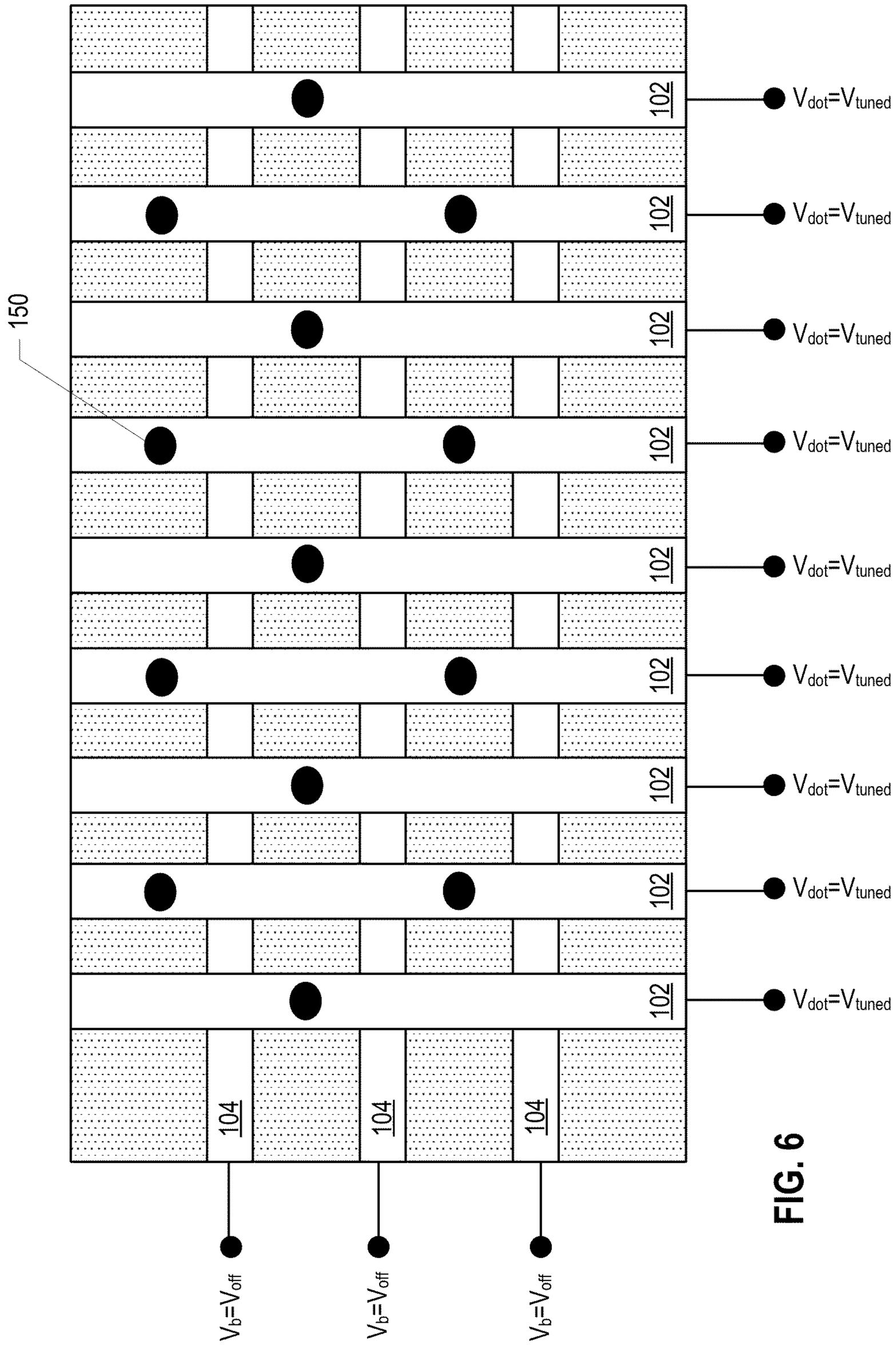


FIG. 5A


150
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$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
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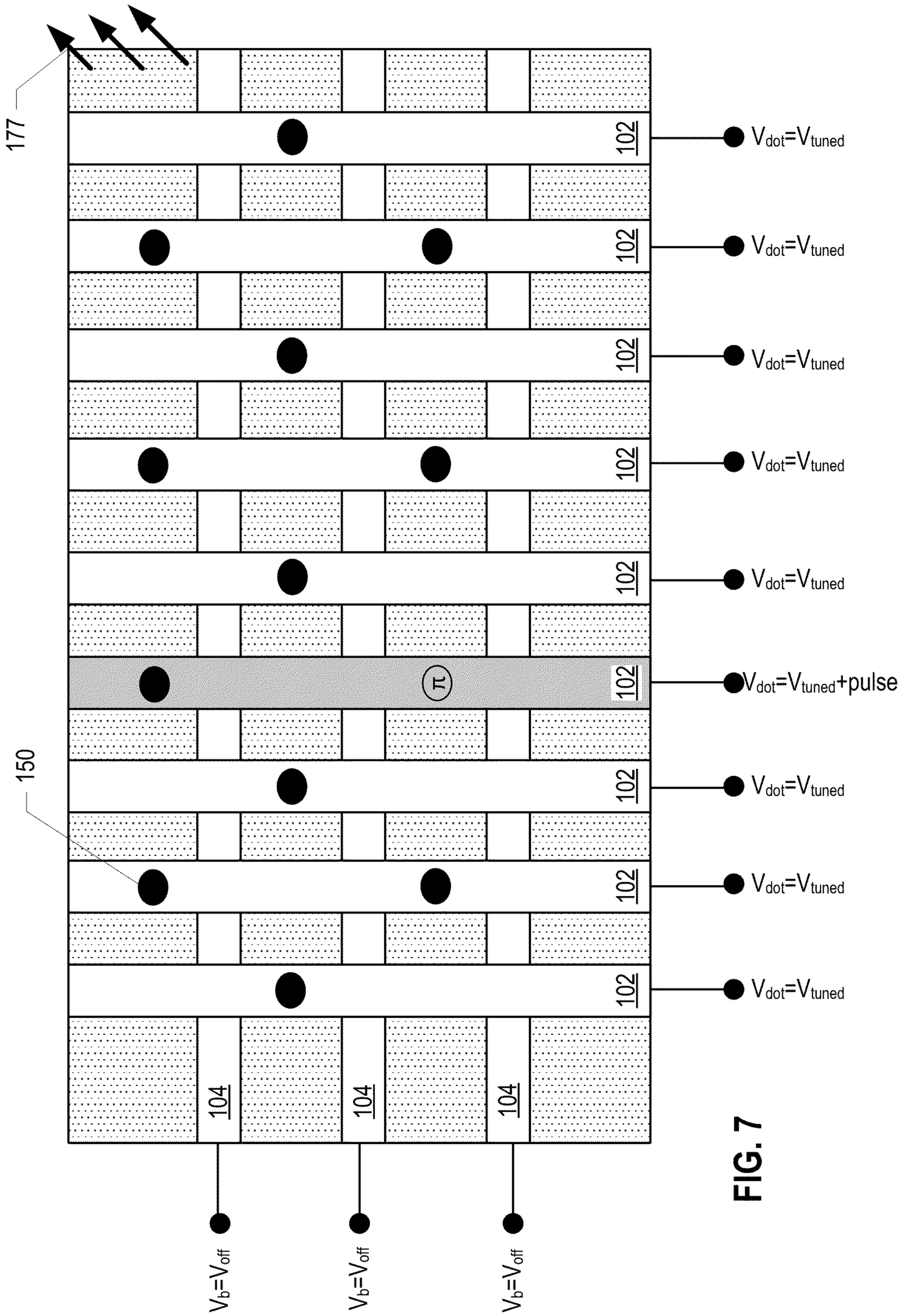
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_b=V_{off}$
$V_b=V_{off}$
$V_b=V_{off}$

FIG. 6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$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
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$V_{dot}=V_{tuned}$
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$V_b=V_{off}$
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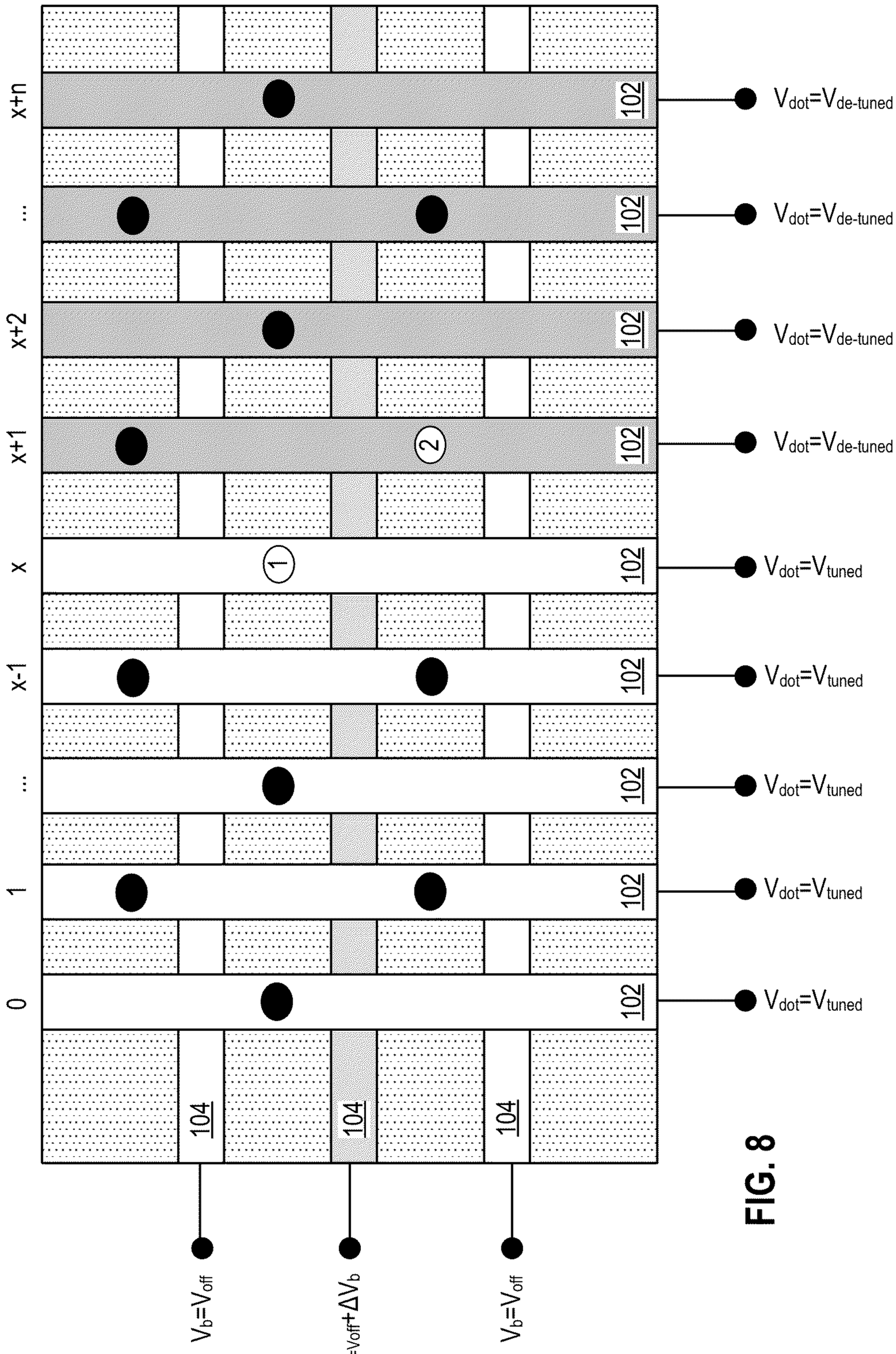
$V_b=V_{off}$

FIG. 7


x+n
...
x+2
x+1
x
x-1
...
1
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102
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104
$V_{dot}=V_{de\text{-}tuned}$
$V_{dot}=V_{tuned}$
$V_b=V_{off}$
$V_b=V_{on=Voff}+\Delta V_b$

FIG. 8

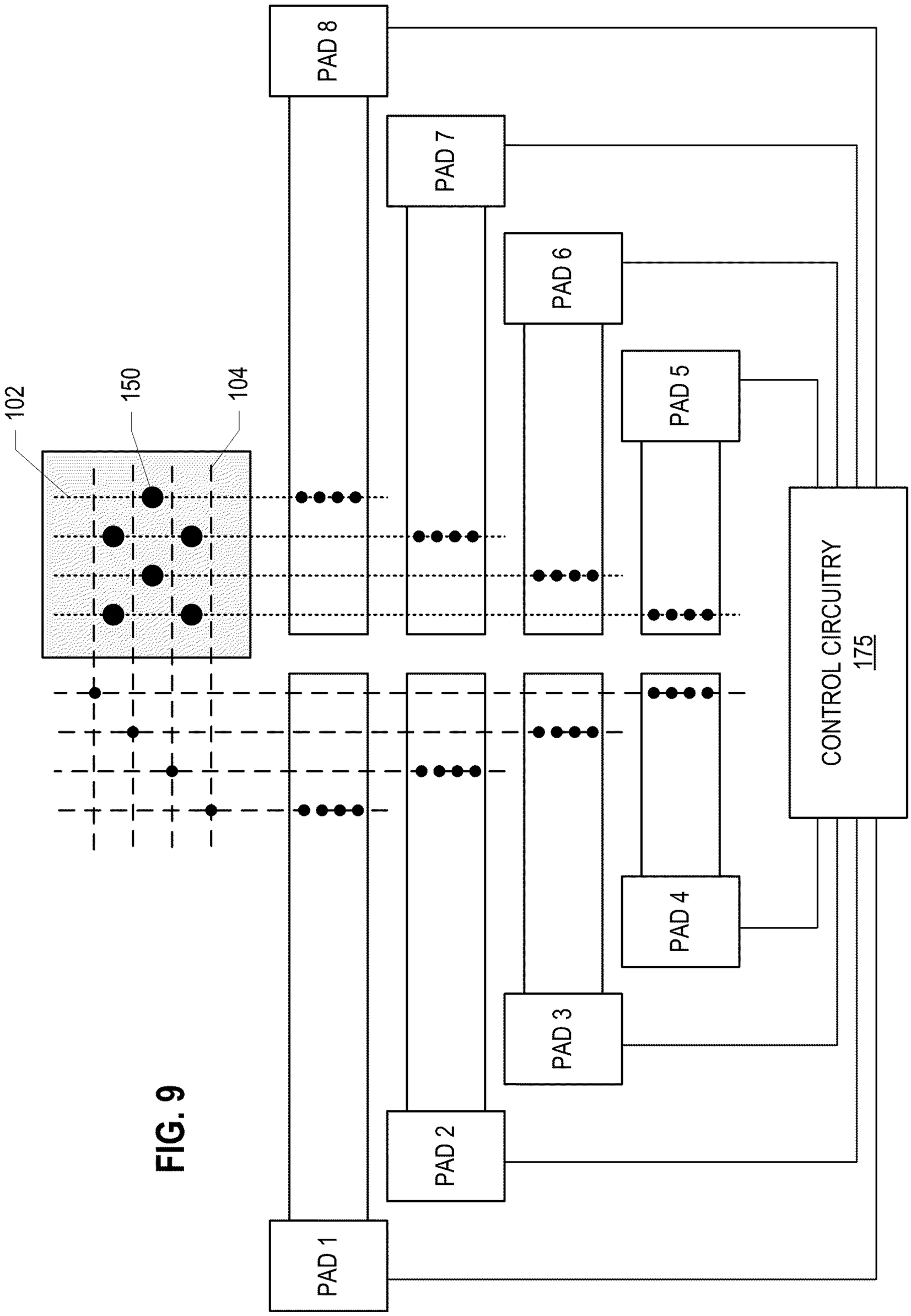
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FIG. 9

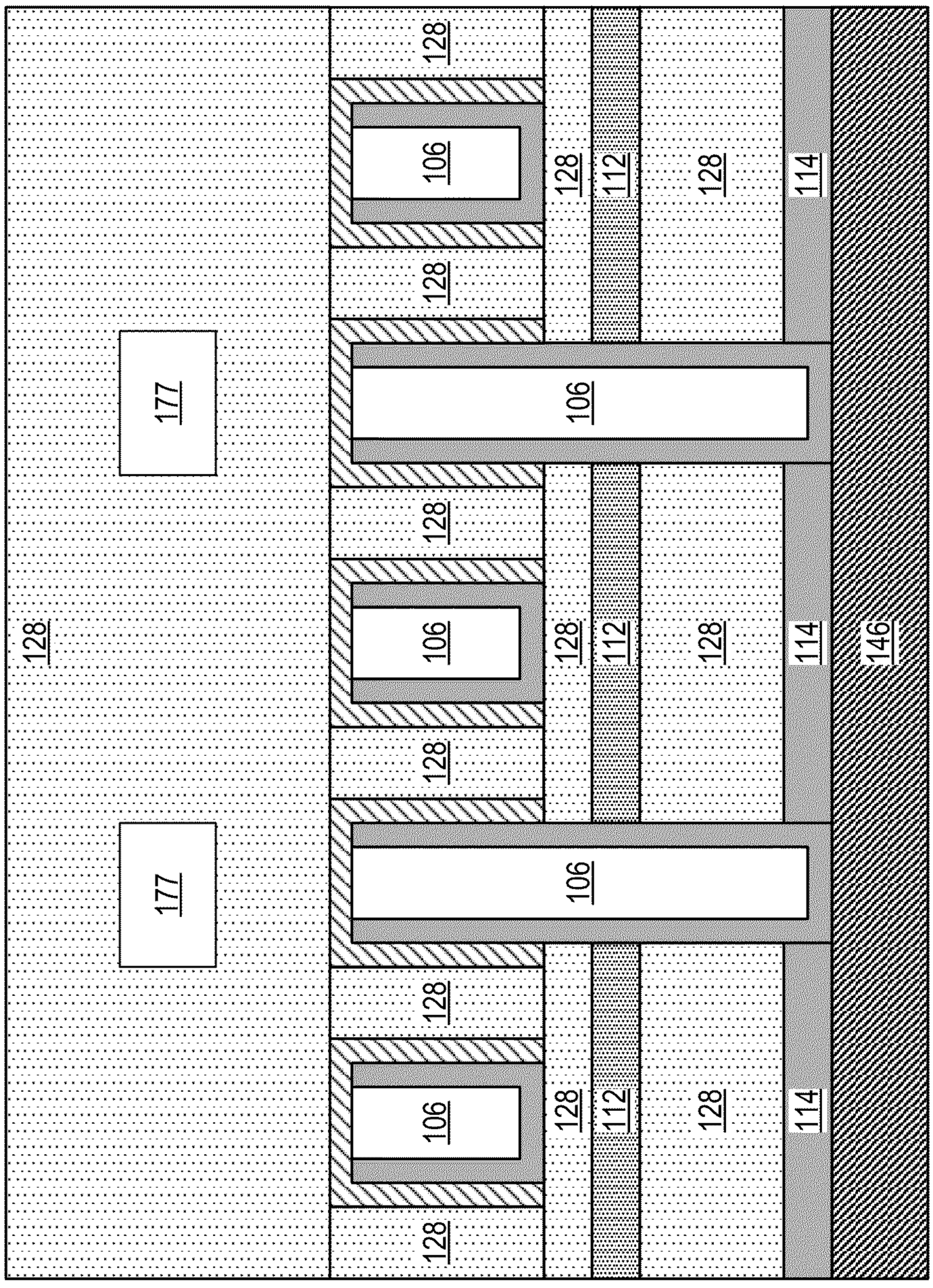
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FIG. 10

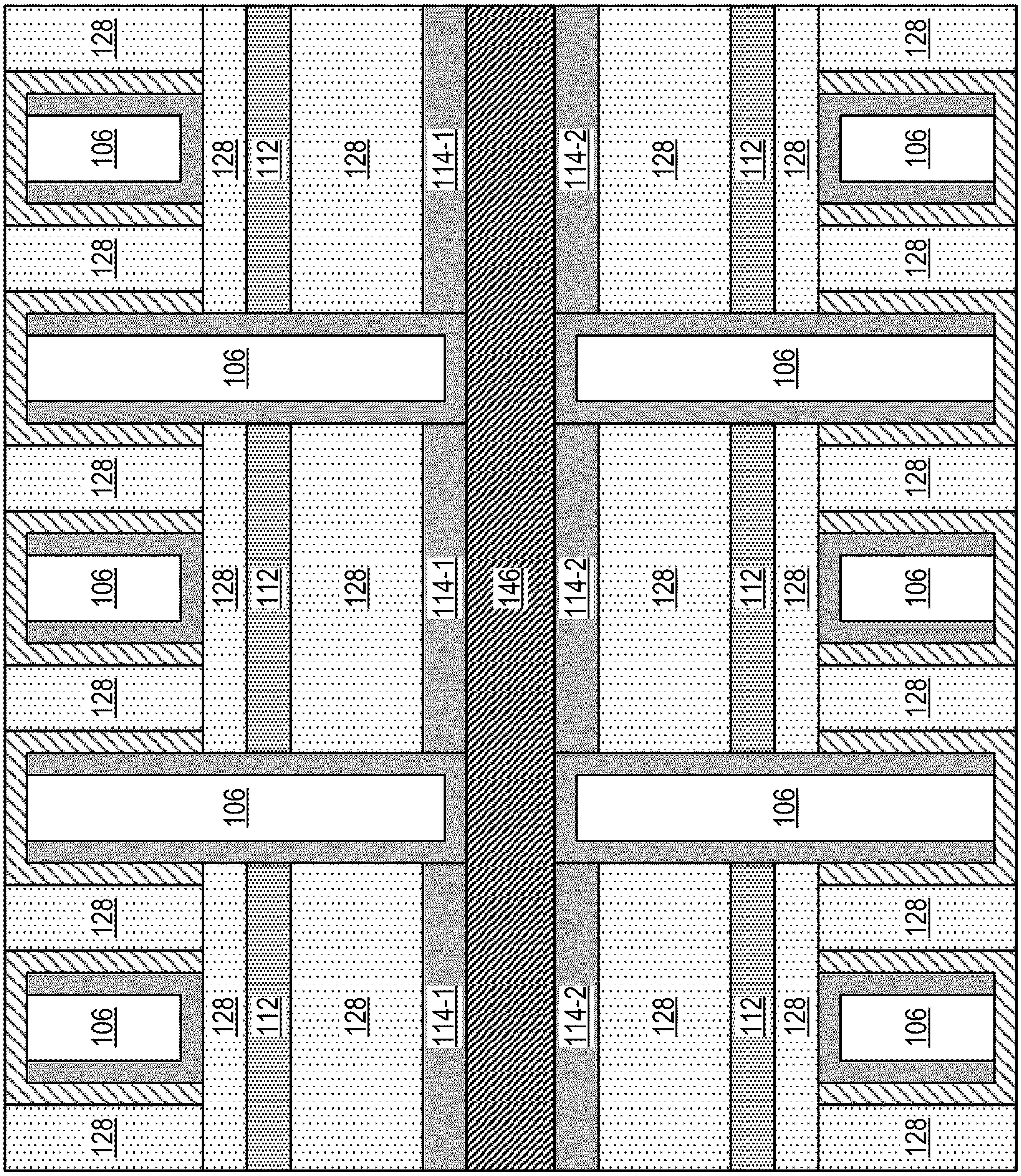

FIG. 11

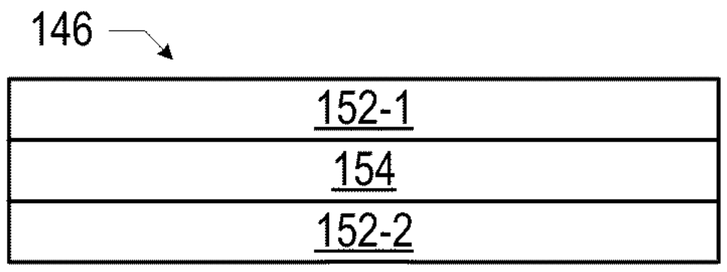

FIG. 12A

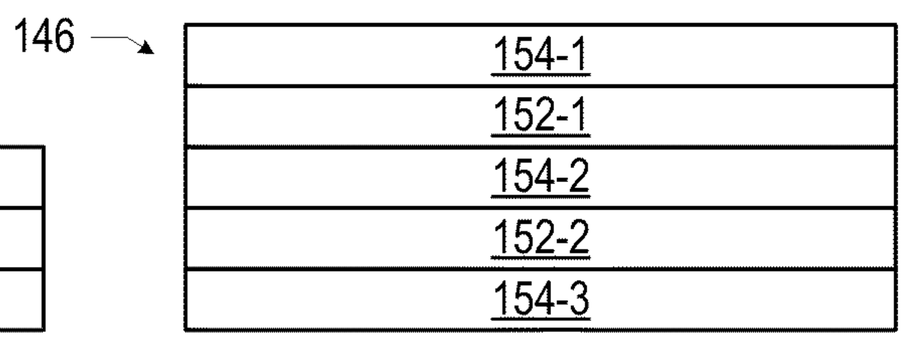

FIG. 12B

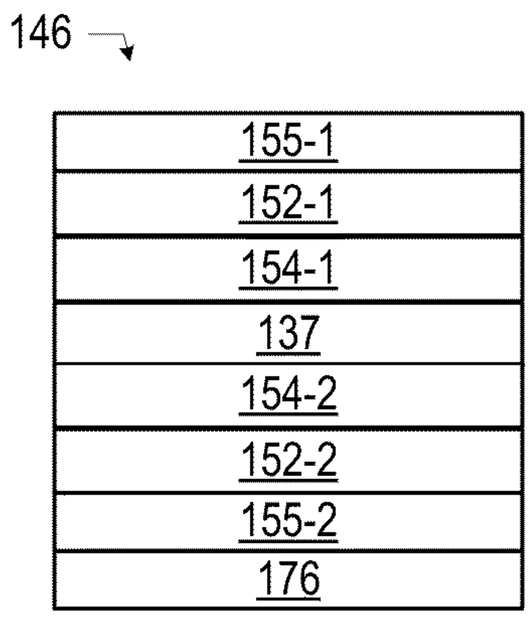

FIG. 12C

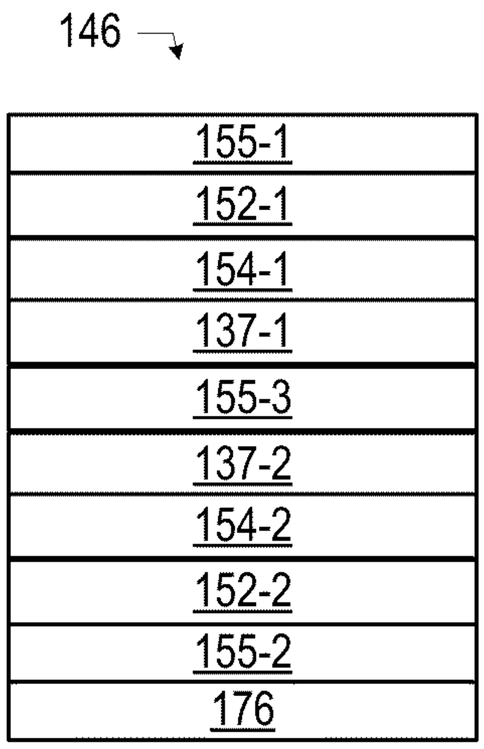

FIG. 12D

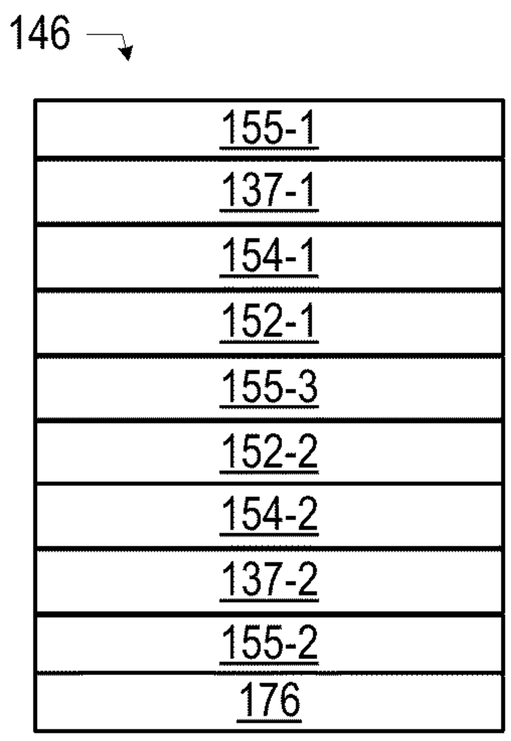

FIG. 12E

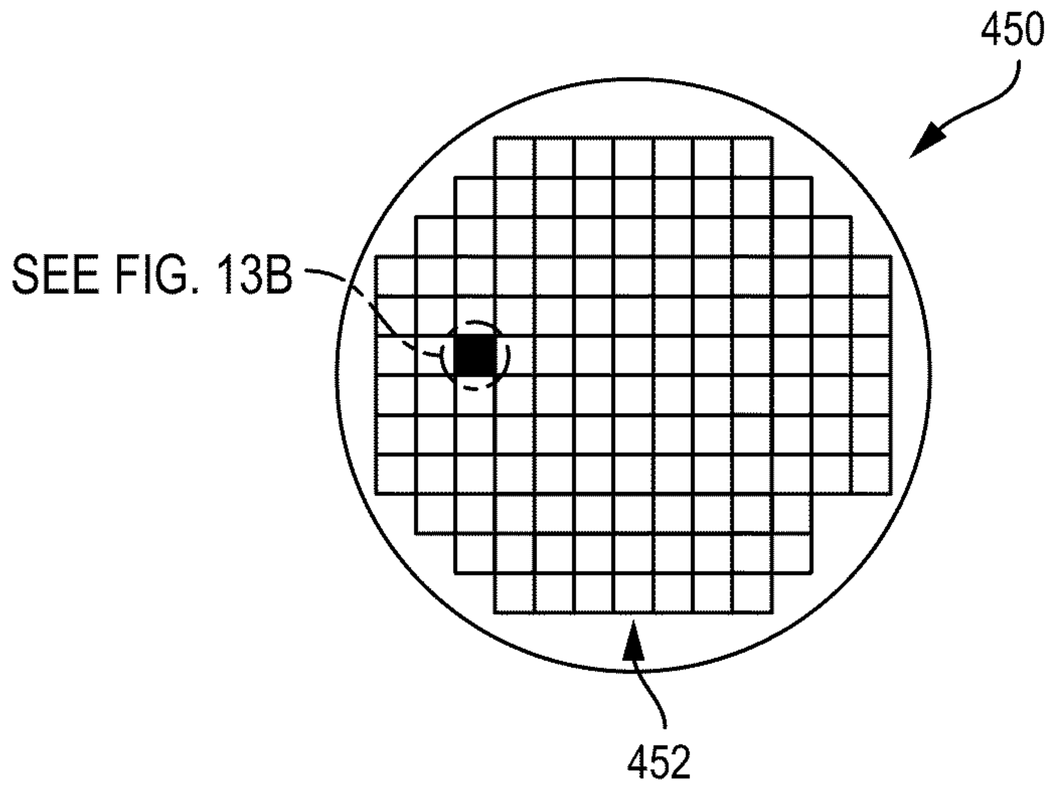

FIG. 13A

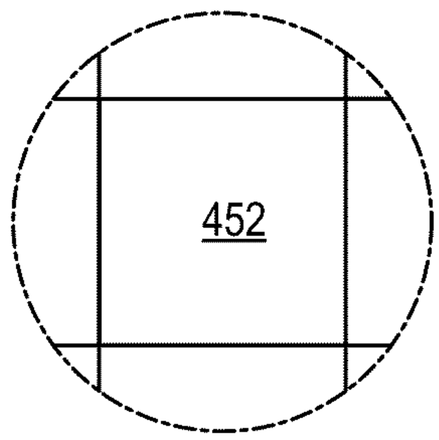

FIG. 13B

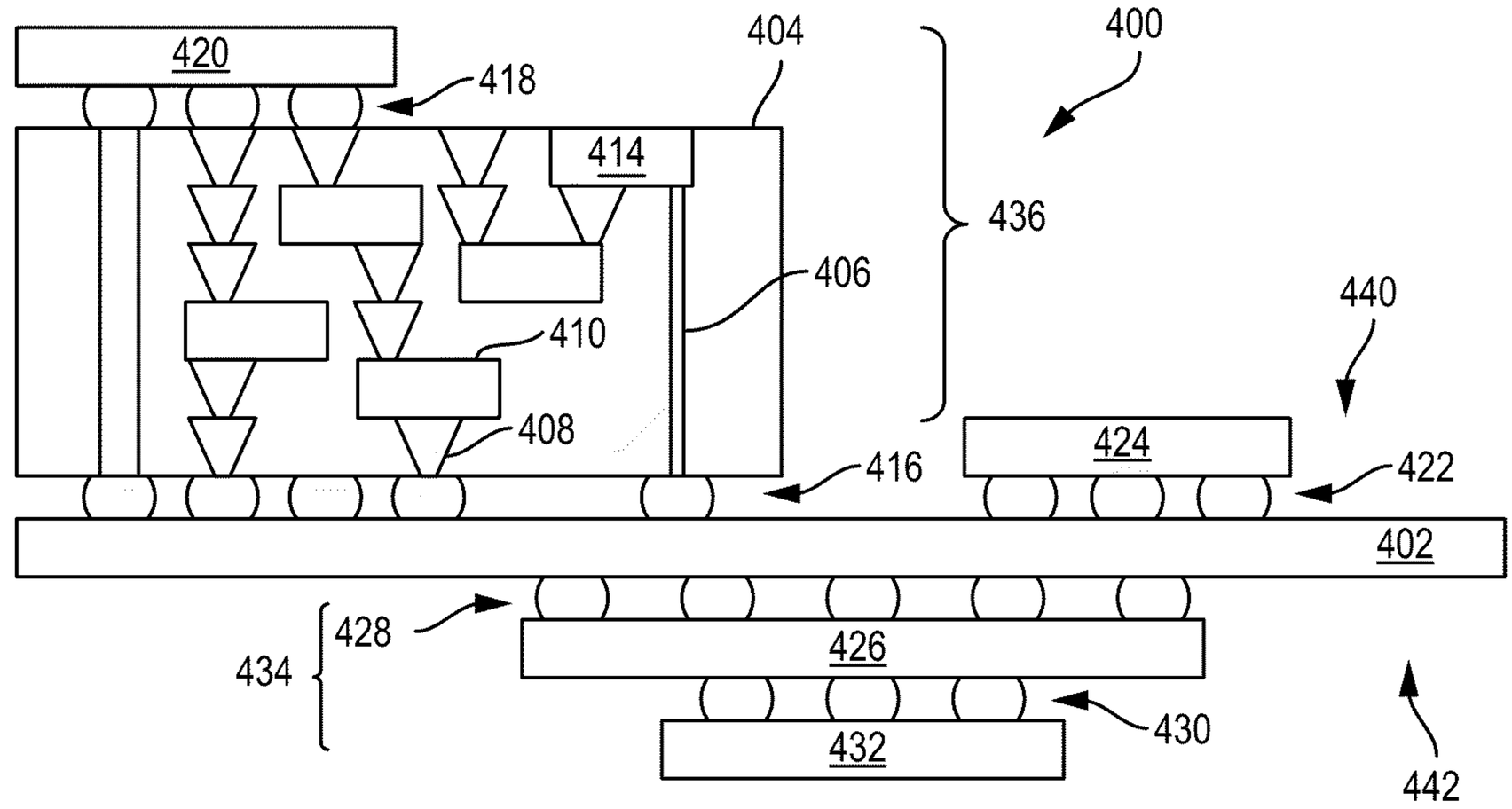

FIG. 14

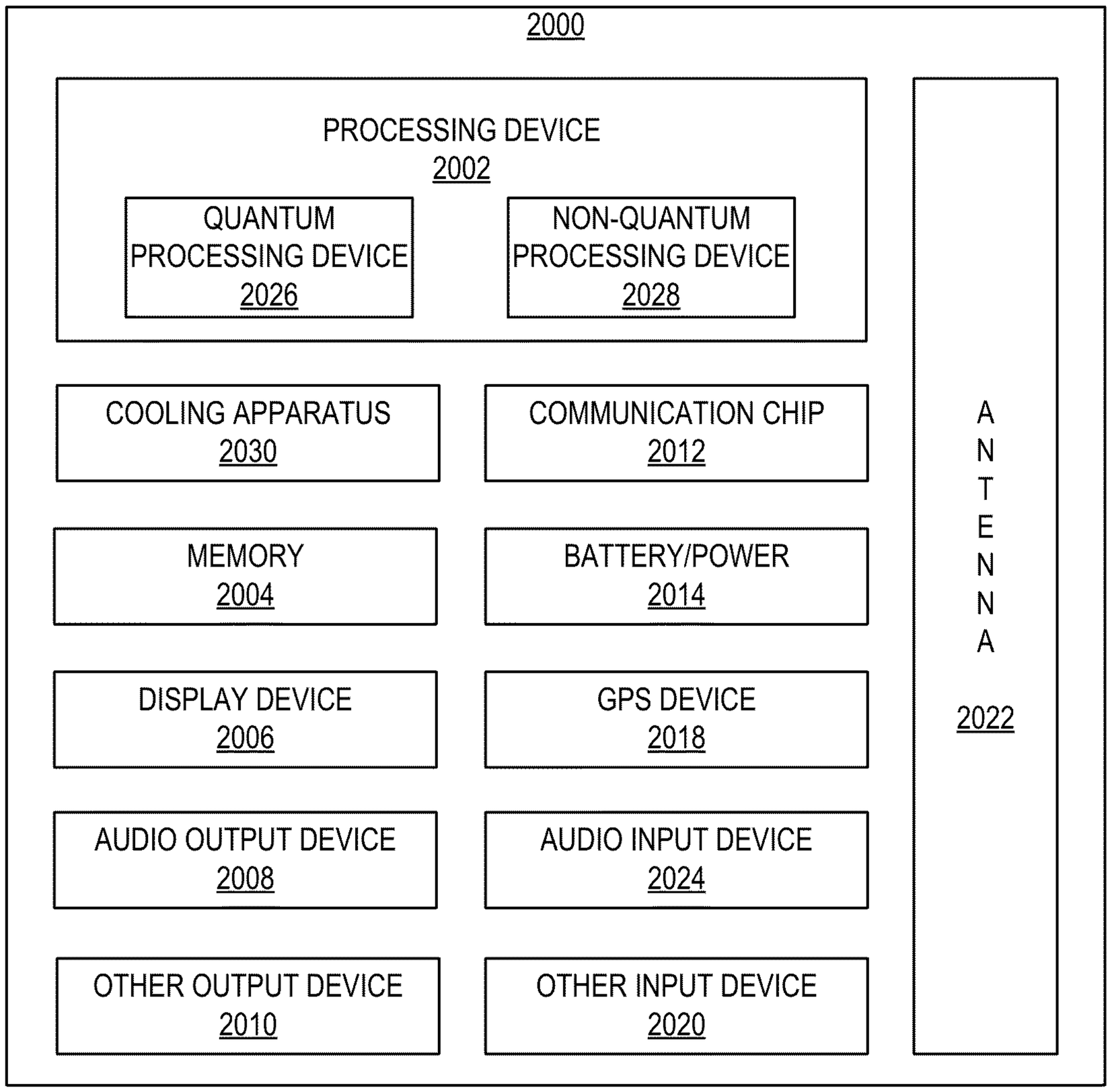
2000
PROCESSING DEVICE
2002
QUANTUM PROCESSING DEVICE
2026
NON-QUANTUM PROCESSING DEVICE
2028
COOLING APPARATUS
2030
COMMUNICATION CHIP
2012
MEMORY
2004
BATTERY/POWER
2014
DISPLAY DEVICE
2006
GPS DEVICE
2018
AUDIO OUTPUT DEVICE
2008
AUDIO INPUT DEVICE
2024
OTHER OUTPUT DEVICE
2010
OTHER INPUT DEVICE
2020
ANTENNA
2022

FIG. 15

QUANTUM DOT DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This Application is a continuation (and claims benefit of priority under 35 U.S.C. §120) of U.S. Application No. 17/341,559 filed Jun. 8, 2021, entitled "QUANTUM DOT DEVICES,", which is a continuation of 16/340,512 filed Apr. 9, 2019, entitled "QUANTUM DOT DEVICES," now U.S. Pat. 11,063,040, which is a 371 of PCT International Application No. PCT/US2016/068603, filed Dec. 24, 2016, entitled "QUANTUM DOT DEVICES," which claims priority to U.S. Provisional Application No. 62/417,047, filed Nov. 3, 2016 entitled "QUANTUM DOT DEVICES." The disclosure of each prior application is considered part of (and is incorporated by reference in) the disclosure of this application.

BACKGROUND

[0002] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIGS. **1**A-**1**E are various views of a quantum dot device, in accordance with various embodiments.

[0005] FIGS. **2**A-**2**U illustrate various example stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0006] FIG. **3** is a view of a quantum dot device, in accordance with various embodiments.

[0007] FIGS. **4**A-**4**D are various views of a quantum dot device, in accordance with various embodiments.

[0008] FIGS. **5**A-**5**C illustrate various example dimensions of a quantum dot device, in accordance with various embodiments.

[0009] FIGS. **6-8** illustrate various electrical configurations that may be used to perform quantum operations on a quantum dot device, in accordance with various embodiments.

[0010] FIG. **9** illustrates an interconnect arrangement for a quantum dot device, in accordance with various embodiments.

[0011] FIG. **10** illustrates an arrangement of magnets associated with quantum dot gates in a quantum dot device, in accordance with various embodiments.

[0012] FIG. **11** illustrates a double-sided quantum dot device, in accordance with various embodiments.

[0013] FIGS. **12**A-**12**E illustrate various embodiments of a quantum well stack that may be included in a quantum dot device, in accordance with various embodiments.

[0014] FIGS. **13**A and **13**B are top views of a wafer and dies that may include any of the quantum dot devices disclosed herein.

[0015] FIG. **14** is a cross-sectional side view of a device assembly that may include any of the quantum dot devices disclosed herein.

[0016] FIG. **15** is a block diagram of an example quantum computing device that may include any of the quantum dot devices disclosed herein, in accordance with various embodiments.

DETAILED DESCRIPTION

[0017] Quantum dot devices, and related systems and methods, are disclosed herein. In some embodiments, a quantum dot device may include a quantum well stack; a plurality of first gates above the quantum well stack; and a plurality of second gates above the quantum well stack; wherein a first gate is between each nearest neighbor pair of second gates. In some embodiments, a quantum dot device may include a quantum well stack; a plurality of first gates above the quantum well stack; and a plurality of second gates above the quantum well stack; wherein the plurality of first gates are arranged in electrically continuous rows extending in a first direction, and the plurality of second gates are arranged in electrically continuous rows extending in a second direction perpendicular to the first direction. In some embodiments, a quantum dot device may include a quantum well stack; a plurality of first gates above the quantum well stack; and a plurality of second gates above the quantum well stack; wherein the plurality of second gates are arranged as points in a grid, and diagonal subsets of the plurality of second gates with respect to the grid are electrically continuous.

[0018] The quantum dot devices disclosed herein may enable the formation of quantum dots to serve as quantum bits ("qubits") in a quantum computing device, as well as the control of these quantum dots to perform quantum logic operations. Unlike previous approaches to quantum dot formation and manipulation, various embodiments of the quantum dot devices disclosed herein provide strong spatial localization of the quantum dots (and therefore good control over quantum dot interactions and manipulation), good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices to integrate the quantum dot devices in larger computing devices.

[0019] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0020] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be per-

formed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0021] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0022] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. As used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide.

[0023] The disclosure may use the singular term "layer," but the term "layer" should be understood to refer to assemblies that may include multiple different material layers. The accompanying drawings are not necessarily drawn to scale. For ease of discussion, all of the lettered sub-figures associated with a particular numbered figure may be referred to by the number of that figure; for example, FIGS. **1**A-**1**E may be referred to as "FIG. **1**," FIGS. **2**A-**2**C may be referred to as "FIG. **2**," etc.

[0024] FIGS. **1**A-**1**E are various views of a quantum dot device **100**, in accordance with various embodiments. FIG. **1**A is a top view of a portion of the quantum dot device **100** with some of the materials removed so that the quantum dot (QD) gate lines and barrier gate lines **104** are visible. Although many of the drawings and description herein may refer to a particular set of lines or gates as "barrier" or "quantum dot" lines or gates, respectively, this is simply for ease of discussion, and in other embodiments, the role of "barrier" and "quantum dot" lines and gates may be switched (e.g., barrier gates may instead act as quantum dot gates, and vice versa). FIGS. **1**B-**1**E are side cross-sectional views of a quantum dot device **100**; in particular, FIG. **1**B is a view through the section B-B of FIG. **1**A, FIG. **1**C is a view through the section C-C of FIG. **1**A, FIG. **1**D is a view through the section D-D of FIG. **1**A, and FIG. **1**E is a view through the section E-E of FIG. **1**A.

[0025] As used herein, during operation of the quantum dot device **100**, electrical signals (e.g., voltages, radio frequency (RF), and/or microwave signals) may be provided to a quantum dot gate (and neighboring gates) to cause a quantum dot (e.g., an electron spin-based quantum dot) to form in a quantum well stack **146** under the quantum dot gate. Electrical signals (e.g., voltages, radio frequency (RF), and/or microwave signals) may be provided to a barrier gate to control the potential energy barrier between adjacent quantum dots.

[0026] In the quantum dot device **100** of FIG. **1**, a gate dielectric **114** is disposed on a quantum well stack **146**. A quantum well stack **146** may include at least one quantum well layer **152** (not shown in FIG. **1**, but discussed below) in which quantum dots may be localized during operation of the quantum dot device **100**; examples of quantum well stacks **146** are discussed below with reference to FIG. **12**. The gate dielectric **114** may be any suitable material, such as a high-k material. Multiple parallel lines of barrier gate metal **108** are disposed on the gate dielectric **114**, and spacer material **118** is disposed on side faces of the barrier gate metal **108**. In some embodiments, a patterned hardmask **110** may be disposed on the barrier gate metal **108** (with the pattern corresponding to the pattern of the barrier gate metal **108**), and the spacer material **118** may extend up the sides of the hardmask **110**, as shown. In some embodiments, an additional hardmask **112** may be disposed on the hardmask **110** (such that there are two hardmasks above the barrier gate metal **108**), and this additional hardmask **112** may be patterned as illustrated in FIG. **1**D to extend over adjacent pairs of barrier gate metal **108** segments. As shown in FIGS. **1**B and **1**D, in some embodiments, additional insulating material **128** (e.g., an interlayer dielectric (ILD)) may be disposed on this additional hardmask **112**. In some embodiments, insulating material **128** (e.g., an ILD) may be disposed between the two hardmasks **110** and **112**. The barrier gate metal **108** may provide barrier gates during operation of the quantum dot device **100**, as discussed below. Different ones of the barrier gate lines **104** may be separately electrically controlled.

[0027] Multiple parallel lines of quantum dot (QD) gate metal may be disposed over the multiple parallel lines of barrier gate metal **108**. As illustrated in FIG. **1**A, the lines of quantum dot gate metal **106** may be arranged perpendicular to the lines of barrier gate metal **108**. As illustrated in FIG. **1**D, the area between adjacent pairs of barrier gate metal **108**/spacer material **118** structures may be alternatingly filled with an insulating material **128** (e.g., an ILD) and the quantum dot gate metal **106**. The quantum dot gate metal **106** may extend over the additional hardmask **112** and additional insulating material **128** above the barrier gate metal **108**, and may extend down into the space between adjacent ones of the barrier gate metal **108**/spacer material **118** structures. The quantum dot gate metal **106** that extends between adjacent ones of the barrier gate metal **108**/spacer material **118** structures may provide a quantum dot gate **150** during operation of the quantum dot device **100** such that quantum dots form in the quantum well stack **146** below the quantum dot gates **150**, as discussed below. The quantum dot gates **150** may alternate with stubs **122** that do not extend as far toward the quantum well stack **146**, as shown. Multiple ones of the quantum dot gates **150** in a quantum dot gate line **102** are electrically continuous due to the continuous quantum dot gate metal **106** over the barrier gates **160**; different ones of the quantum dot gate lines **102** may be separately electrically controlled. As illustrated in FIGS. **1**B and **1**C, upper portions of the quantum dot gate lines **102** may have spacer material **118** disposed on the top and side faces. Different portions of the quantum dot gate metal **106** may also have gate dielectric **114** disposed on the bottom and side faces, as shown.

[0028] Although FIG. **1** illustrates a particular number of quantum dot gate lines **102** and barrier gate lines **104**, this is simply for illustrative purposes, and any number of quantum dot gate lines **102** and barrier gate lines **104** may be included in a quantum dot device **100**. Other examples of quantum

dot gate line **102** and barrier gate line **104** arrangements are discussed below with reference to FIGS. **3**, **4**, and **6-8**. Electrical interconnects (e.g., vias and conductive lines) may make contact with the quantum dot gate lines **102** and barrier gate lines **104** in any desired manner; some example arrangements are discussed below with reference to FIG. **9**. Examples of methods of performing quantum operations with the quantum dot device **100** of FIG. **1** (or similar devices) are discussed below with reference to FIGS. **6-8**.

[0029] Not illustrated in FIG. **1**, but illustrated in FIG. **4**, are accumulation regions **162** that may be electrically coupled to the quantum well layer of the quantum well stack **146**. The accumulation regions **162** may be regions in which carriers accumulate (e.g., due to doping, or due to the presence of large electrodes that pull carriers into the quantum well layer), and may serve as reservoirs of carriers that can be selectively drawn into the areas of the quantum well layer under the quantum dot gates (e.g., by controlling the voltages on the quantum dot gates and the barrier gates **160**) to form carrier-based quantum dots (e.g., electron or hole quantum dots). In other embodiments (e.g., as discussed below with reference to FIG. **12**), a quantum dot device **100** may not include lateral accumulation regions **162**, but may instead include doped layers within the quantum well stack **146**. These doped layers may provide the carriers to the quantum well layer. Any combination of accumulation regions **162** (e.g., doped or non-doped) or doped layers in a quantum well stack **146** may be used in any of the embodiments of the quantum dot devices **100** disclosed herein.

[0030] FIGS. **2**A-**2**U illustrate various example stages in the manufacture of a quantum dot device **100**, in accordance with various embodiments. The views illustrated in FIGS. **2**A-**2**H are taken along the cross section of FIG. **1**D, the view illustrated in FIG. **2**I is a top view similar to the top view of FIG. **1**A, and the views illustrated in FIGS. **2**J-**2**U are taken along the cross section of FIG. **1**C.

[0031] FIG. **2**A illustrates an assembly including a quantum well stack **146**, a gate dielectric **114** disposed on the quantum well stack **146**, a barrier gate metal **108** disposed on the gate dielectric **114**, a hardmask **110** disposed on the barrier gate metal **108**, a template material **132** disposed on the hardmask **110**, and a patterned photoresist **130** disposed on the template material **132**. The photoresist **130** may be any suitable material, and may be patterned using any suitable technique. In some embodiments, the template material **132** may be amorphous silicon, or any other suitable material.

[0032] FIG. **2**B illustrates an assembly subsequent to patterning the template material **132** of the assembly of FIG. **2**A in accordance with the pattern of the photoresist **130**, then removing the photoresist **130**. Any suitable etch process may be used to pattern the template material **132**.

[0033] FIG. **2**C illustrates an assembly subsequent to providing spacer material **134** on side faces of the patterned template material **132** of the assembly of FIG. **2**B. The spacer material **134** of FIG. **2**C may be formed by depositing a conformal layer of the spacer material **134** over the patterned template material **132**, then performing a directional etch to etch the spacer material **134** "downward," leaving the spacer material **134** on the sides of the patterned template material **132**. The spacer material **134** may be an insulating material, for example.

[0034] FIG. **2**D illustrates an assembly subsequent to removing the template material **132** from the assembly of FIG. **2**C. The template material **132** may be removed using any suitable etch process.

[0035] FIG. **2**E illustrates an assembly subsequent to etching the hardmask **110** and the barrier gate metal **108** of the assembly of FIG. **2**D in accordance with the pattern provided by the spacer material **134** (i.e., the hardmask **110** and barrier gate metal **108** not masked by the spacer material **134** may be removed). Any suitable etch process may be used to pattern the hardmask **110** and the barrier gate metal **108**. In some embodiments, as shown, the etch may stop at the gate dielectric **114**, while in other embodiments, the etch may continue through the gate dielectric **114**.

[0036] FIG. **2**F illustrates an assembly subsequent to removing the spacer material **134** of the assembly of FIG. **2**E. Any suitable technique may be used.

[0037] FIG. **2**G illustrates an assembly subsequent to providing spacer material **118** on side faces of the patterned hardmask **110** and barrier gate metal **108** of the assembly of FIG. **2**F. The spacer material **118** of FIG. **2**G may be formed using the techniques discussed above with reference to FIG. **2**C, for example.

[0038] FIG. **2**H illustrates an assembly subsequent to providing an insulating material **128** on the assembly of FIG. **2**G. The insulating material **128** may be, for example, an ILD. In some embodiments, the insulating material **128** may fill the area above the gate dielectric **114** between adjacent portions of spacer material **118** and extend over the hardmask **110**, as shown. In some embodiments, the insulating material **128** may be planarized after deposition (e.g., using a chemical mechanical polishing (CMP) technique). FIG. **2**I is a "top" view of the assembly of FIG. **2**H, with some of the insulating material **128** removed to show the barrier gate lines **104**.

[0039] FIG. **2**J is a cross-sectional view through the dashed line of FIG. **2**I, subsequent to providing an additional hardmask **112** on the insulating material **128** of FIG. **2**I, as well as providing additional insulating material **128**, template material **136**, and a patterned photoresist **138**. The additional insulating material **128** may take the form of any of the insulating materials **128** discussed above with reference to FIG. **2**H. The additional hardmask **112** may take the form of any of the hardmasks discussed above with reference to FIG. **2**A. The template material **136** and patterned photoresist **138** may take the form of any of the template materials and patterned photoresists, respectively, discussed above with reference to FIG. **2**A.

[0040] FIG. **2**K illustrates an assembly subsequent to patterning the template material **136** of the assembly of FIG. **2**J in accordance with the pattern of the photoresist **138**, then removing the photoresist **138**. Any suitable etch process may be used to pattern the template material **136**.

[0041] FIG. **2**L illustrates an assembly subsequent to providing spacer material **140** on side faces of the patterned template material **136** of the assembly of FIG. **2**K. The spacer material **140** of FIG. **2**L may be formed using the techniques discussed above with reference to FIG. **2**C, for example.

[0042] FIG. **2**M illustrates an assembly subsequent to removing the template material **136** from the assembly of FIG. **2**L. The template material **136** may be removed using any suitable etch process.

[0043] FIG. **2**N illustrates an assembly subsequent to depositing additional template material **144** on the assembly of FIG. **2**M, planarizing that additional template material **144**, and depositing additional photoresist **148** on the additional template material **144**. The additional photoresist **148** may be deposited using any suitable technique, such as spin coating.

[0044] FIG. **2**O illustrates an assembly subsequent to forming openings in the photoresist **148** of the assembly of FIG. **2**N to expose alternating portions of the additional template material **144**, as shown. The openings may be formed using via lithography, or any other suitable process, and may have a circular cross section when viewed from above.

[0045] FIG. **2**P illustrates an assembly subsequent to etching the additional template material **144**, the insulating material **128**, the gate dielectric **114**, and the additional hardmask **112** in accordance with the pattern provided by the patterned photoresist **148** and spacer material **140** (i.e., the additional template material **144**, the insulating material **128**, the gate dielectric **114**, and the additional hardmask **112** not masked by the photoresist **148** or the spacer material **140** may be removed). Any suitable etch process may be used to pattern the additional template material **144**, the additional hardmask **112**, the gate dielectric **114**, and the insulating material **128**. In some embodiments, as shown, the etch may continue through the gate dielectric **114**, while in other embodiments, the etch may stop without removing any of the gate dielectric **114**.

[0046] FIG. **2**Q illustrates an assembly subsequent to removing the photoresist **148** and the additional template material **144** of the assembly of FIG. **2**P. Any suitable technique may be used.

[0047] FIG. **2**R illustrates an assembly subsequent to depositing a conformal gate dielectric **114** over the assembly of FIG. **2**Q, followed by the deposition and planarization of the quantum dot gate metal **106** (e.g., by CMP). The assembly of FIG. **2**R thus includes alternating stubs **122** (which may not provide gate functionality during operation) and quantum dot gates **150** (which extend closer to the quantum well stack **146**, and thus may provide gate functionality during operation).

[0048] FIG. **2**S illustrates an assembly subsequent to removing the spacer material **140** of the assembly of FIG. **2**R. Any suitable technique may be used.

[0049] FIG. **2**T illustrates an assembly subsequent to providing spacer material **118** on the assembly of FIG. **2**S. In some embodiments, the spacer material **118** may be conformal, and may be directionally etched as discussed previously. In some embodiments, some of the spacer material **118** may remain on "top" of the quantum dot gate metal **106**, as well as on the side faces of the quantum dot gate metal **106**.

[0050] FIG. **2**U illustrates an assembly subsequent to providing an insulating material **128** on the assembly of FIG. **2**T. The insulating material **128** may be, for example, an ILD. In some embodiments, the insulating material **128** may fill the area above the insulating material **128** between adjacent portions of spacer material **118**. In some embodiments, the insulating material **128** may be planarized after deposition (e.g., using CMP). The assembly of FIG. **2**U may take the form of the quantum dot device **100** illustrated in FIG. **1**.

[0051] FIG. **3** is a view of a quantum dot device **100**, in accordance with various embodiments. In particular, FIG. **3** schematically illustrates a quantum dot device **100** having a two-dimensional arrangement of barrier gates **160** and quantum dot gates **150**. In some embodiments, the quantum dot device **100** schematically illustrated in FIG. **3** may take the form of any of the quantum dot devices **100** discussed above with reference to FIGS. **1** and **2**. In such embodiments, multiple ones of the barrier gates **160** illustrated in FIG. **3** as connected by a barrier gate line **104** may physically take the form of a single elongated barrier gate, as discussed above with reference to FIG. **3**, while multiple ones of the quantum dot gates **150** illustrated in FIG. **3** as connected by a quantum dot gate line **102** may take the form of an electrically continuous structure having alternating quantum dot gates **150** and stubs **122**, as discussed above.

[0052] In FIG. **3**, barrier gates **160** arranged along a barrier gate line **104** are electrically continuous, and thus any voltage applied to a barrier gate line **104** will be applied to all of the barrier gates **160** along that line. Similarly, quantum dot gates **150** arranged along a quantum dot gate line **102** are electrically continuous, and thus any voltage applied to a quantum dot gate line **102** will be applied to all of the quantum dot gates **150** along that line. In the quantum dot device **100** of FIG. **3**, the barrier gate lines **104** are parallel to each other, the quantum dot gate lines **102** are parallel to each other, and the barrier gate lines **104** are perpendicular to the quantum dot gate lines **102**.

[0053] The quantum dot gates **150** in the quantum dot device **100** of FIG. **3** (and the quantum dot devices **100** of FIGS. **1** and **4**-**9**) are arranged as points in a grid, and different ones of the quantum dot gate lines **102** are electrically coupled to different diagonals in that grid. The barrier gates **160** in the quantum dot device **100** of FIG. **3** (and the quantum dot devices **100** of FIGS. **1** and **4**-**9**) are arranged as points in a grid, and different ones of the barrier gate lines **104** are electrically coupled to different rows in that grid. The grid underlying the quantum dot gates **150** is rotated 45 degrees with reference to the grid underlying the barrier gates **160**.

[0054] In the quantum dot device **100** of FIG. **3**, the quantum dot gates **150** in each nearest neighbor pair have a barrier gate disposed between them. The quantum dot gate lines **102** connect quantum dot gates **150** along the diagonal of the underlying grid. As discussed in further detail below, during operation of the quantum dot device **100** of FIG. **3**, quantum interactions between nearest neighbor quantum dots under different ones of the quantum dot gates **150** may be controlled in part by the potential energy barrier provided by the intervening barrier gates **160**.

[0055] FIGS. **4**A-**4**D are various views of a quantum dot device **100**, in accordance with various embodiments. In particular, FIG. **4**A is a "top" view similar to the views of FIGS. **1**A and **3**, FIG. **4**B is a cross-sectional view corresponding to the arrow marked "B" in FIG. **4**A, FIG. **4**C is a cross-sectional view similar to that of FIG. **1**B (and corresponding to the arrow marked "C" in FIG. **4**A), and FIG. **4**D is a cross-sectional view similar to that of FIG. **1**D (and corresponding to the arrow marked "D" in FIG. **4**A). The embodiment illustrated in FIG. **4** is substantially similar to that discussed above with reference to FIGS. **1** and **2**, except that the gate dielectric **114** does not extend continuously over the quantum well stack **146**, but is instead separately disposed between different portions of the gate metals and the quantum well stack **146**. Such an arrangement may be manufactured by not initially depositing a gate dielectric

114, and instead depositing the gate dielectric **114** just prior to depositing the gate metal. FIGS. **4**B-**4**D also include some example dimensions for example embodiments of the quantum dot devices **100** disclosed herein, as well as illustrating the location of quantum dots **142** (shown as "e-" electron-spin-based quantum dots) under the quantum dot gates **150**. In some embodiments, the distance **164** may be between 50 nanometers and 200 nanometers (e.g., between 75 and 125 nanometers, between 80 and 90 nanometers, or approximately 84 nanometers). In some embodiments, the distance **166** may be between 25 and 100 nanometers (e.g., between 40 and 80 nanometers, or approximately 70 nanometers). In some embodiments, the distance **168** may be between 80 and 200 nanometers (e.g., between **100** and 150 nanometers, or approximately 120 nanometers). Comparing FIGS. **4**B and **4**D, nearest neighbor quantum dots (e.g., on the "diagonal") may be substantially closer together than quantum dots under adjacent quantum dot gates in a single quantum dot gate line **102**, and thus the nearest neighbor quantum dots may be close enough to interact (while those under adjacent quantum dot gates in a single quantum dot gate line **102** may not be close enough to interact). Quantum operations using the quantum dot devices **100** disclosed herein may thus be said to take place "on the diagonal," as discussed in further detail below.

[0056] FIGS. **5**A-**5**C illustrate various example dimensions of a quantum dot device **100**, in accordance with various embodiments. For example, as illustrated in FIG. **5**A, when the quantum dot gate lines **102** have a pitch of 60 nanometers, and the barrier gate lines **104** have a pitch of 60 nanometers, two quantum dots that form under nearest neighbor quantum dot gates (along the "diagonal") may be spaced apart by approximately 85 nanometers. As illustrated in FIG. **5**B, when the quantum dot gate lines **102** have a pitch of 45 nanometers, and the barrier gate lines **104** have a pitch of 45 nanometers, two quantum dots that form under nearest neighbor quantum dot gates may be spaced apart by approximately 64 nanometers. As illustrated in FIG. **5**C, when the quantum dot gate lines **102** have a pitch of 60 nanometers, and the barrier gate lines **104** have a pitch of 45 nanometers (or vice versa), two quantum dots that form under nearest neighbor quantum dot gates may be spaced apart by approximately 75 nanometers. Any other desired pitches or combinations of pitches may be used to pattern the quantum dot gate lines **102** and/or the barrier gate lines **104**.

[0057] FIGS. **6-8** illustrate various electrical configurations that may be used to perform quantum operations in a quantum dot device **100**, in accordance with various embodiments. The quantum dot device **100** schematically illustrated in FIGS. **6-8** may take the form of any of the quantum dot devices **100** disclosed herein (e.g., any of those discussed above with reference to FIGS. **1-5**). The voltages applied to the gate lines, as discussed below with reference to FIGS. **6-8**, may be controlled by any suitable control circuitry **175** (illustrated in FIG. **9**). The control circuitry **175** may include multiplexers or other suitable circuitry for selectively applying voltages to various ones of the gate lines. In particular, the control circuitry **175** may be configured to provide an adjustable voltage to a selected barrier gate line **104** while leaving other barrier gate lines **104** at a constant voltage, as suitable. The control circuitry **175** may also be configured to provide microwave pulses and DC voltage to each quantum dot gate line **102** separately, and hold DC voltages constant during operation, as suitable.

[0058] FIG. **6** illustrates an electrical configuration in which quantum dots are formed under quantum dot gates (indicated by the green circles), but no quantum dot interactions take place. In the configuration of FIG. **6**, all of the quantum dot gate lines **102** may be supplied with voltages (indicated as Vtuned) in FIG. **6** that allow the quantum dot gates associated with different quantum dot gate lines **102** to be at essentially similar energy levels, and thus not likely to engage in quantum interaction across different quantum dot gate lines **102**. Note that the particular voltage value corresponding to Vtuned for a particular quantum dot gate line **102** may be different from the particular voltage value corresponding to Vtuned for a different quantum dot gate line **102**; however, the voltages on each of the quantum dot gate lines **102** may be set to a "tuned" value (that may differ between quantum dot gate lines **102**) that limits or prevents quantum interaction between quantum dots forming under the different quantum dot gate lines **102**. Similarly, the barrier gate lines **104** may be supplied with voltages (indicated as Voff) that may be sufficient to provide a high potential energy barrier between the quantum dot gates on either side of the barrier gate lines **104**. Note that the particular voltage value corresponding to Voff for a particular barrier gate line **104** may be different than the particular voltage value corresponding to Voff for another barrier gate line **104**; however, the voltages on each of the barrier gate lines **104** may be set to an "off" value (that may differ between barrier gate lines **104**) that limits or prevents quantum interaction between quantum dots forming on either side of each barrier gate line **104**. The sequence of voltages applied to the quantum dot and barrier gate lines **104** may allow each of the quantum dots to be occupied by a single electron, and, as noted above, the voltage Voff on the barrier gate lines **104** may be sufficient to provide a high potential energy barrier between nearest neighbor quantum dots and thereby limit or prevent quantum interaction.

[0059] FIG. **7** illustrates an electrical configuration that may implement a Pauli gate (or "NOT") operation on a particular quantum dot (identified in FIG. **7** by "π"). In some embodiments, the quantum dot device **100** may include a set of magnets **177** above the quantum dot gates such that the quantum dot gates are disposed between corresponding magnets **177** and the quantum well stack **146**. The magnets **177** may be magnets, for example. FIG. **10** illustrates one example arrangement of magnets **177** in a quantum dot device **100**, but any desired arrangement may be used. Each magnet **177** along a quantum dot gate line **102** may have a different associated frequency. This frequency may be engineered to take a particular value, or different magnets **177** may have different frequencies due to process variations. Any suitable magnets **177** may be used, and each magnet **177** may thus act as an "antenna" for directing energy of a matching frequency to the quantum dot associated with the magnet **177**. To perform a Pauli gate operation, a microwave pulse (e.g., in the gigahertz range) may be applied to the quantum dot gate line **102** that includes the quantum dot gate associated with the quantum dot π. The frequency of the microwave pulse may allow the quantum dot π to be selected by the field gradient of the associated magnet **177**, and thus the microwave pulse may change only the state of the quantum dot π (and not other quantum dots disposed below the same quantum dot gate line **102**). The

voltages on the other quantum dot gate lines **102** may remain fixed, and the voltages on the barrier gate lines **104** may also remain fixed to confine the Pauli gate operation to the quantum dot π.

[0060] FIG. **8** illustrates an electrical configuration that may implement an exchange gate operation on a pair of nearest neighbor ("diagonal") quantum dots (identified in FIG. **8** by "1" and "2"). An exchange gate may allow the quantum dots 1 and 2 to undergo a quantum interaction by appropriately adjusting the potential energy around them, as described below. The barrier gate line **104** that separates the quantum dots 1 and 2 may have its voltage adjusted to a value (Von) that lowers the potential energy barrier between the quantum dots 1 and 2 low enough for them to interact; other barrier gate lines **104** may maintain voltages (Voff) in which quantum dots separated by the associated barrier gates **160** do not interact (as discussed above with reference to FIG. **6**). The voltage applied to the quantum dot gate line **102** associated with quantum dot 1 (labeled gate line "x") and the voltage applied to the quantum dot gate line **102** associated with quantum dot 2 (labeled gate line "x+1") may be made different from each other to provide some energy for their interaction. All of the quantum dot gate lines **102** on the same "side" as the quantum dot gate line **102** x (i.e., the quantum dot gate lines **102** 0,...,x-1) may have mutually tuned voltages (which may differ between different quantum dot gate lines **102**, as discussed above with reference to FIG. **6**) that tunes these quantum dot gate lines **102** to the quantum dot gate line **102** x (in FIG. **8**, indicated as Vtuned) so that quantum dots formed under different ones of these quantum dot gate lines **102** 0,..., x may not interact. Similarly, all of the quantum dot gate lines **102** on the same "side" as the quantum dot gate line **102** x+1 (i.e., the quantum dot gate lines **102** x+2,...,x+n) may have mutually tuned voltages (which may differ between different quantum dot gate lines **102**, as discussed above with reference to FIG. **6**) that tunes these quantum dot gate lines **102** to the quantum dot gate line **102** x+1 (in FIG. **8**, indicated as Vde-tuned) so that quantum dots formed under different ones of the quantum dot gate lines **102** x+1,...,x+n may not interact. In this manner, the interaction of quantum dots in the quantum dot device **100** of FIG. **8** may be limited to the interaction of quantum dots 1 and 2. Any pair of nearest neighbor quantum dots may be selectively allowed to interact using such a technique.

[0061] FIG. **9** illustrates an interconnect arrangement for a quantum dot device **100**, in accordance with various embodiments. The quantum dot device **100** schematically illustrated in FIG. **9** may take the form of any of the quantum dot devices **100** disclosed herein (e.g., those discussed above with reference to FIGS. **1-5**), and interconnects may be made to the barrier gate lines **104** and the quantum dot gate lines **102** in any desired manner. In FIG. **9**, each gate line may be routed out to a bond pad for connection to a processing device or other control device to control the voltages on the gate lines (e.g., to perform any of the operations discussed above with reference to FIGS. **6-8**).

[0062] FIG. **11** is a cross-sectional view of a double-sided quantum dot device **100**, in accordance with various embodiments. The quantum dot device **100** of FIG. **11** may be formed by performing the operations discussed above with reference to FIG. **2**, flipping the result over, and performing the same operations on the "other side" of the quantum well stack **146**. The quantum well stack **146** may itself include two quantum well layers, one in which quantum dots may be formed by the gates on the corresponding side of the quantum well stack **146**, and the other in which quantum dots may be formed by the gates on the other, corresponding side of the quantum well stack **146**. In some embodiments, the quantum dots formed in one of the quantum well layers may act as the "active" quantum dots in the quantum dot device **100**, and the quantum dots formed in the other of the quantum well layers may act as the "read" quantum dots, sensing the state of the active quantum dots for readout (e.g., through the corresponding gates and other interconnects).

[0063] FIGS. **12**A-**12**E illustrate various examples of quantum well stacks **146** that may provide the quantum well stacks **146** of any of the embodiments of the quantum dot devices **100** disclosed herein. In some embodiments, the layers of the quantum well stacks **146** may be grown on a substrate (e.g., a silicon or germanium wafer) (and on each other) by epitaxy. Although the quantum well stacks **146** illustrated in FIG. **12** each include two quantum well layers **152** (e.g., as appropriate for a double-sided device, as discussed above with reference to FIG. **11**), in some embodiments, the quantum well stack **146** included in a quantum dot device **100** may include one quantum well layer **152** or more than two quantum well layers **152**; elements may be omitted from the quantum well stacks **146**, or added to the quantum well stacks **146**, discussed with reference to FIG. **12** to achieve such embodiments, as appropriate. Layers other than the quantum well layer(s) **152** in a quantum well stack **146** may have higher threshold voltages for conduction than the quantum well layer(s) **152** so that when the quantum well layer(s) **152** are biased at their threshold voltages, the quantum well layer(s) **152** conduct and the other layers of the quantum well stack **146** do not. This may avoid parallel conduction in both the quantum well layer(s) **152** and the other layers, and thus avoid compromising the strong mobility of the quantum well layer(s) **152** with conduction in layers having inferior mobility.

[0064] FIG. **12**A is a cross-sectional view of a quantum well stack **146** including only a quantum well layer **152-1**, a barrier layer **154**, and a quantum well layer **152-2**. In some embodiments, the quantum well layers **152** of FIG. **12**A may be formed of intrinsic silicon, and the gate dielectrics **114** may be formed of silicon oxide; in such an arrangement, during use of the quantum dot device **100**, a 2DEG may form in the intrinsic silicon at the interface between the intrinsic silicon and the proximate silicon oxide. Embodiments in which the quantum well layers **152** of FIG. **12**A are formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices **100**. In some embodiments, the quantum well layers **152** of FIG. **12**A may be formed of intrinsic germanium, and the gate dielectrics **114** may be formed of germanium oxide; in such an arrangement, during use of the quantum dot device **100**, a 2DEG may form in the intrinsic germanium at the interface between the intrinsic germanium and the proximate germanium oxide. Such embodiments may be particularly advantageous for hole-type quantum dot devices **100**. In some embodiments, the quantum well layers **152** may be strained, while in other embodiments, the quantum well layers **152** may not be strained.

[0065] The barrier layer **154** of FIG. **12**A may provide a potential barrier between the quantum well layer **152-1** and the quantum well layer **152-2**. In some embodiments in

which the quantum well layers **152** of FIG. **12**A are formed of silicon, the barrier layer **154** may be formed of silicon germanium. The germanium content of this silicon germanium may be 20-80% (e.g., 30%). In some embodiments in which the quantum well layers **152** are formed of germanium, the barrier layer **154** may be formed of silicon germanium (with a germanium content of 20-80% (e.g., 70%)).

[0066] The thicknesses (i.e., z-heights) of the layers in the quantum well stack **146** of FIG. **12**A may take any suitable values. For example, in some embodiments, the thickness of the barrier layer **154** (e.g., silicon germanium) may be between 0 and 400 nanometers. In some embodiments, the thickness of the quantum well layers **152** (e.g., silicon or germanium) may be between 5 and 30 nanometers.

[0067] FIG. **12**B is a cross-sectional view of a quantum well stack **146** including quantum well layers **152-1** and **152-2**, a barrier layer **154-2** disposed between the quantum well layers **152-1** and **152-2**, and additional barrier layers **154-1** and **154-3**. In the quantum dot device **100**, the barrier layer **154-1** may be disposed between the quantum well layer **152-1** and the gate dielectric **114-1** (see, e.g., FIG. **11**). The barrier layer **154-3** may be disposed between the quantum well layer **152-2** and the gate dielectric **114-2** (see, e.g., FIG. **11**). In some embodiments, the barrier layer **154-3** may be formed of a material (e.g., silicon germanium), and when the quantum well stack **146** is being grown on the substrate **144**, the barrier layer **154-3** may include a buffer region of that material. This buffer region may trap defects that form in this material as it is grown on the substrate **144**, and in some embodiments, the buffer region may be grown under different conditions (e.g., deposition temperature or growth rate) from the rest of the barrier layer **154-3**. In particular, the rest of the barrier layer **154-3** may be grown under conditions that achieve fewer defects than the buffer region. In some embodiments, the buffer region may be lattice mismatched with the quantum well layer(s) **152** in a quantum well stack **146**, imparting biaxial strain to the quantum well layer(s) **152**.

[0068] The barrier layers **154-1** and **154-3** may provide potential energy barriers around the quantum well layers **152-1** and **152-2**, respectively, and the barrier layer **154-1** may take the form of any of the embodiments of the barrier layer **154-3** discussed herein. In some embodiments, the barrier layer **154-1** may have a similar form as the barrier layer **154-3**, but may not include a "buffer region" as discussed above; in the quantum dot device **100**, the barrier layer **154-3** and the barrier layer **154-1** may have substantially the same structure. The barrier layer **154-2** may take the form of any of the embodiments of the barrier layer **154** discussed above with reference to FIG. **12**A. The thicknesses (i.e., z-heights) of the layers in the quantum well stack **146** of FIG. **12**B may take any suitable values. For example, in some embodiments, the thickness of the barrier layers **154-1** and **154-3** (e.g., silicon germanium) in the quantum dot device **100** may be between 0 and 400 nanometers. In some embodiments, the thickness of the quantum well layers **152** (e.g., silicon or germanium) may be between 5 and 30 nanometers (e.g., 10 nanometers). In some embodiments, the thickness of the barrier layer **154-2** (e.g., silicon germanium) may be between 25 and 75 nanometers (e.g., 32 nanometers).

[0069] FIGS. **12**C-**12**D illustrate examples of quantum well stacks **146** including doped layer(s) **137**. As noted above, doped layer(s) **137** may be included in a quantum well stack **146** instead of or in addition to an accumulation region **162**.

[0070] FIG. **12**C is a cross-sectional view of a quantum well stack **146** including a buffer layer **176**, a barrier layer **155-2**, a quantum well layer **152-2**, a barrier layer **154-2**, a doped layer **137**, a barrier layer **154-1**, a quantum well layer **152-1**, and a barrier layer **155-1**.

[0071] The buffer layer **176** may be formed of the same material as the barrier layer **155-2**, and may be present to trap defects that form in this material as it is grown. In some embodiments, the buffer layer **176** may be grown under different conditions (e.g., deposition temperature or growth rate) from the barrier layer **155-2**. In particular, the barrier layer **155-2** may be grown under conditions that achieve fewer defects than the buffer layer **176**. In some embodiments in which the buffer layer **176** includes silicon germanium, the silicon germanium of the buffer layer **176** may have a germanium content that varies to the barrier layer **155-2**; for example, the silicon germanium of the buffer layer **176** may have a germanium content that varies from zero percent to a nonzero percent (e.g., 30%) at the barrier layer **155-2**. The buffer layer **176** may be grown beyond its critical layer thickness such that it is substantially free of stress from the underlying base (and thus may be referred to as "relaxed"). In some embodiments, the thickness of the buffer layer **176** (e.g., silicon germanium) may be between 0.3 and 4 microns (e.g., 0.3-2 microns, or 0.5 microns). In some embodiments, the buffer layer **176** may be lattice mismatched with the quantum well layer(s) **152** in a quantum well stack **146**, imparting biaxial strain to the quantum well layer(s) **152**.

[0072] The barrier layer **155-2** may provide a potential energy barrier proximate to the quantum well layer **152-2**. The barrier layer **155-2** may be formed of any suitable materials. For example, in some embodiments in which the quantum well layer **152** is formed of silicon or germanium, the barrier layer **155-2** may be formed of silicon germanium. In some embodiments, the thickness of the barrier layer **155-2** may be between 0 and 400 nanometers (e.g., between 25 and 75 nanometers).

[0073] The quantum well layer **152-2** may be formed of a different material than the barrier layer **155-2**. Generally, a quantum well layer **152** may be formed of a material such that, during operation of the quantum dot device **100**, a 2DEG may form in the quantum well layer **152**. Embodiments in which the quantum well layer **152** is formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices **100**. Embodiments in which a quantum well layer **152** is formed of intrinsic germanium may be particularly advantageous for hole-type quantum dot devices **100**. In some embodiments, a quantum well layer **152** may be strained, while in other embodiments, a quantum well layer **152** may not be strained. The thickness of a quantum well layer **152** may take any suitable values; in some embodiments, a quantum well layer **152** may have a thickness between 5 and 30 nanometers.

[0074] In the quantum well stack **146** of FIG. **12**C, the doped layer **137** may be "shared" by the two quantum well layers **152** in the quantum well stack **146**, in that the doped layer **137** provides carriers to the quantum well layer **152-1** and the quantum well layer **152-2** during use. In the quantum dot device **100**, the quantum well layer **152-1** may be disposed between the doped layer **137** and the gate dielectric **114-1**, while the quantum well layer **152-2** may be disposed

between the doped layer **137** and the gate dielectric **114-2**. The doped layer **137** of FIG. **12**C may be doped with an n-type material (e.g., for an electron-type quantum dot device **100**) or a p-type material (e.g., for a hole-type quantum dot device **100**). In some embodiments, the doping concentration of the doped layer **137** may be between $10^{17}/cm^3$ and $10^{20}/cm^3$ (e.g., between $10^{17}/cm^3$ and $10^{18}/cm^3$). The thickness (i.e., z-height) of the doped layer **137** may depend on the doping concentration, among other factors, and in some embodiments, may be between 5 and 50 nanometers (e.g., between 20 and 30 nanometers).

[0075] A doped layer **137** may be formed using any of a number of techniques. In some embodiments, a doped layer **137** may be formed of an undoped base material (e.g., silicon germanium) that is doped in situ during growth of the base material by epitaxy. In some embodiments, a doped layer **137** may initially be fully formed of an undoped base material (e.g., silicon germanium), then a layer of dopant may be deposited on this base material (e.g., a monolayer of the desired dopant), and an annealing process may be performed to drive the dopant into the base material. In some embodiments, a doped layer **137** may initially be fully formed of an undoped base material (e.g., silicon germanium), and the dopant may be implanted into the lattice (and, in some embodiments, may be subsequently annealed). In some embodiments, a doped layer **137** may be provided by a silicon germanium layer (e.g., with 90% germanium content) doped with an n-type dopant. In general, any suitable technique may be used to form a doped layer **137**.

[0076] The barrier layer **154-2** may not be doped, and thus may provide a barrier to prevent impurities in the doped layer **137** from diffusing into the quantum well layer **152-2** and forming recombination sites or other defects that may reduce channel conduction and thereby impede performance of the quantum dot device **100**. In some embodiments of the quantum well stack **146** of FIG. **12**C, the doped layer **137** may include a same material as the barrier layer **154-2**, but the barrier layer **154-2** may not be doped. For example, in some embodiments, the doped layer **137** and the barrier layer **154-2** may both be silicon germanium. In some embodiments in which the quantum well layer **152-2** is formed of silicon, the barrier layer **154-2** may be formed of silicon germanium. The germanium content of this silicon germanium may be 20-80% (e.g., 30%). In some embodiments in which the quantum well layer **152-2** is formed of germanium, the barrier layer **154-2** may be formed of silicon germanium (with a germanium content of 20-80% (e.g., 70%)). The thickness of the barrier layer **154-2** may depend on the doping concentration of the doped layer **137**, among other factors discussed below, and in some embodiments, may be between 5 and 50 nanometers (e.g., between 20 and 30 nanometers).

[0077] The barrier layer **154-1** may provide a barrier to prevent impurities in the doped layer **137** from diffusing into the quantum well layer **152-1**, and may take any of the forms described herein for the barrier layer **154-2**. Similarly, the quantum well layer **152-1** may take any of the forms described herein for the quantum well layer **152-2**. The barrier layer **155-1** may provide a potential energy barrier proximate to the quantum well layer **152-1** (as discussed above with reference to the barrier layer **155-2** and the quantum well layer **152-2**), and may take any of the forms described herein for the barrier layer **155-2**.

[0078] The thickness of a barrier layer **154** may impact the ease with which carriers in the doped layer **137** can move into a quantum well layer **152** disposed on the other side of the barrier layer **154**. The thicker the barrier layer **154**, the more difficult it may be for carriers to move into the quantum well layer **152**; at the same time, the thicker the barrier layer **154**, the more effective it may be at preventing impurities from the doped layer **137** from moving into the quantum well layer **152**. Additionally, the diffusion of impurities may depend on the temperature at which the quantum dot device **100** operates. Thus, the thickness of the barrier layer **154** may be adjusted to achieve a desired energy barrier and impurity screening effect between the doped layer **137** and the quantum well layer **152** during expected operating conditions.

[0079] In some embodiments of the quantum well stack **146** of FIG. **12**C (e.g., those included in "single-sided" quantum dot devices **100**), only a single quantum well layer **152** may be included. For example, the layers **154-1** and **152-1** may be omitted, and gates may be formed proximate to the barrier layer **155-1** such that the quantum well layer **152-1** is disposed between the gates and the doped layer **137**. In other embodiments, the layers **154-1**, **152-1**, and **155-2** may be omitted, and gates may be formed proximate to the doped layer **137**. In some embodiments, the buffer layer **176** and/or the barrier layer **155-2** may be omitted from the quantum well stack **146** of FIG. **12**C.

[0080] FIG. **12**D is a cross-sectional view of a quantum well stack **146** that is similar to the quantum well stack **146** of FIG. **12**C, except that in the place of the single doped layer **137** shared by two quantum well layers **152**, the quantum well stack **146** of FIG. **12**D includes two different doped layers **137-2** and **137-1** (spaced apart by a barrier layer **155-3**). In such an embodiment, the doped layer **137-2** may provide a source of carriers for the quantum well layer **152-2**, and the doped layer **137-1** may provide a source of carriers for the quantum well layer **152-1**. The barrier layer **155-3** may provide a potential barrier between the two doped layers **137**, and may take any suitable form. Generally, the elements of the quantum well stack **146** of FIG. **12**D may take the form of any of the corresponding elements of the quantum well stack **146** of FIG. **12**C. The doped layers **137-1** and **137-2** may have the same geometry and material composition, or may have different geometries and/or material compositions.

[0081] FIG. **12**E is a cross-sectional view of a quantum well stack **146** in which two doped layers **137-1** and **137-2** are disposed toward the "outside" of the quantum well stack **146**, rather than the "inside" of the quantum well stack **146**, as illustrated in FIGS. **12**C and **12**D. In particular, the quantum well layer **152-2** is disposed between the doped layer **137-2** and the quantum well layer **152-1**, and the quantum well layer **152-1** is disposed between the doped layer **137-1** and the quantum well layer **152-2**. In the quantum dot device **100**, the doped layer **137-1** may be disposed between the quantum well layer **152-1** and the gate dielectric **114-1**, while the doped layer **137-2** may be disposed between the quantum well layer **152-2** and the gate dielectric **114-2**. In the quantum well stack **146** of FIG. **12**E, a barrier layer **155-3** provides a potential barrier between the quantum well layers **152-1** and **152-2** (rather than between the doped layers **137-1** and **137-2**, as illustrated in the quantum well stack **146** of FIG. **12**D). Generally, the elements of the quantum well stack **146** of FIG. **12**E may take the form of any of

the corresponding elements of the quantum well stack **146** of FIGS. **12**A-D.

[0082] In some particular embodiments in which the quantum dot device **100** is a "single-sided" device with only one set of gates, the quantum well stack **146** may include a silicon base, a buffer layer **176** of silicon germanium (e.g., with 30% germanium content), then a doped layer **137** formed of silicon germanium doped with an n-type dopant, a thin barrier layer **154** formed of silicon germanium (e.g., silicon germanium with 70% germanium content), a silicon quantum well layer **152**, and a barrier layer **155** formed of silicon germanium (e.g., with 30% germanium content); in such an embodiment, the gates may be disposed on the barrier layer **155**. In some other particular embodiments in which the quantum dot device **100** is a "single-sided" device with only one set of gates, the quantum well stack **146** may include a silicon base, a doped layer **137** formed of silicon doped with an n-type dopant, a thin barrier layer **154** formed of silicon germanium, and a silicon quantum well layer **152**; in such an embodiment, the gates may be disposed on the silicon quantum well layer **152**.

[0083] FIGS. **13**A-B are top views of a wafer **450** and dies **452** that may be formed from the wafer **450**; the dies **452** may include any of the quantum dot devices **100** disclosed herein. The wafer **450** may include semiconductor material and may include one or more dies **452** having conventional and quantum dot device elements formed on a surface of the wafer **450**. Each of the dies **452** may be a repeating unit of a semiconductor product that includes any suitable conventional and/or quantum dot device. After the fabrication of the semiconductor product is complete, the wafer **450** may undergo a singulation process in which each of the dies **452** is separated from one another to provide discrete "chips" of the semiconductor product. A die **452** may include one or more quantum dot devices **100** and/or supporting circuitry to route electrical signals to the quantum dot devices (e.g., interconnects including conductive vias and lines, or any control circuitry **175**, as discussed above with reference to FIG. **9**), as well as any other IC components. In some embodiments, the wafer **450** or the die **452** may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die **452**. For example, a memory array formed by multiple memory devices may be formed on a same die **452** as a processing device (e.g., the processing device **2002** of FIG. **15**) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0084] FIG. **14** is a cross-sectional side view of a device assembly **400** that may include any of the embodiments of the quantum dot devices **100** disclosed herein. The device assembly **400** includes a number of components disposed on a circuit board **402**. The device assembly **400** may include components disposed on a first face **440** of the circuit board **402** and an opposing second face **442** of the circuit board **402**; generally, components may be disposed on one or both faces **440** and **442**.

[0085] In some embodiments, the circuit board **402** may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board **402**. In other embodiments, the circuit board **402** may be a package substrate or flexible board.

[0086] The device assembly **400** illustrated in FIG. **14** includes a package-on-interposer structure **436** coupled to the first face **440** of the circuit board **402** by coupling components **416**. The coupling components **416** may electrically and mechanically couple the package-on-interposer structure **436** to the circuit board **402**, and may include solder balls (as shown in FIG. **14**), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0087] The package-on-interposer structure **436** may include a package **420** coupled to an interposer **404** by coupling components **418**. The coupling components **418** may take any suitable form for the application, such as the forms discussed above with reference to the coupling components **416**. Although a single package **420** is shown in FIG. **14**, multiple packages may be coupled to the interposer **404**; indeed, additional interposers may be coupled to the interposer **404**. The interposer **404** may provide an intervening substrate used to bridge the circuit board **402** and the package **420**. The package **420** may be a quantum dot device package (e.g., a package that includes one or more quantum dot devices **100**) or may be a conventional lC package, for example. In some embodiments, the package **420** may include a quantum dot device die (e.g., a die that includes one or more quantum dot devices **100**) coupled to a package substrate (e.g., by flip chip connections). Generally, the interposer **404** may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer **404** may couple the package **420** (e.g., a die) to a ball grid array (BGA) of the coupling components **416** for coupling to the circuit board **402**. In the embodiment illustrated in FIG. **14**, the package **420** and the circuit board **402** are attached to opposing sides of the interposer **404**; in other embodiments, the package **420** and the circuit board **402** may be attached to a same side of the interposer **404**. In some embodiments, three or more components may be interconnected by way of the interposer **404**.

[0088] The interposer **404** may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer **404** may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer **404** may include metal interconnects **408** and vias **410**, including but not limited to through-silicon vias (TSVs) **406**. The interposer **404** may further include embedded devices **414**, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer **404**. The package-on-interposer structure **436** may take the form of any of the package-on-interposer structures known in the art.

[0089] The device assembly **400** may include a package **424** coupled to the first face **440** of the circuit board **402** by coupling components **422**. The coupling components **422** may take the form of any of the embodiments discussed above with reference to the coupling components **416**, and the package **424** may take the form of any of the embodiments discussed above with reference to the package **420**. The package **424** may be a quantum dot device package (e.g., a package that includes one or more quantum dot devices **100**) or may be a conventional lC package, for example. In some embodiments, the package **424** may include a quantum dot device die (e.g., a die that includes one or more quantum dot devices **100**) coupled to a package substrate (e.g., by flip chip connections).

[0090] The device assembly **400** illustrated in FIG. **14** includes a package-on-package structure **434** coupled to the second face **442** of the circuit board **402** by coupling components **428**. The package-on-package structure **434** may include a package **426** and a package **432** coupled together by coupling components **430** such that the package **426** is disposed between the circuit board **402** and the package **432**. The coupling components **428** and **430** may take the form of any of the embodiments of the coupling components **416** discussed above, and the packages **426** and **432** may take the form of any of the embodiments of the package **420** discussed above. Each of the packages **426** and **432** may be a quantum dot device package (e.g., a package that includes one or more quantum dot devices **100**) or may be a conventional lC package, for example. In some embodiments, one or both of the packages **426** and **432** may take the form of any of the embodiments of a quantum dot device package (e.g., a package that includes one or more quantum dot devices **100**) disclosed herein, and may include a die coupled to a package substrate (e.g., by flip chip connections).

[0091] FIG. **15** is a block diagram of an example quantum computing device **2000** that may include any of the quantum dot devices **100** disclosed herein. A number of components are illustrated in FIG. **15** as included in the quantum computing device **2000**, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device **2000** may be attached to one or more printed circuit boards (e.g., a motherboard). In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device **2000** may not include one or more of the components illustrated in FIG. **15**, but the quantum computing device **2000** may include interface circuitry for coupling to the one or more components. For example, the quantum computing device **2000** may not include a display device **2006**, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device **2006** may be coupled. In another set of examples, the quantum computing device **2000** may not include an audio input device **2024** or an audio output device **2008**, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device **2024** or audio output device **2008** may be coupled.

[0092] The quantum computing device **2000** may include a processing device **2002** (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device **2002** may include a quantum processing device **2026** (e.g., one or more quantum processing devices), and a non-quantum processing device **2028** (e.g., one or more non-quantum processing devices). The quantum processing device **2026** may include one or more of the quantum dot devices **100** disclosed herein, and may perform data processing by performing operations on the quantum dots that may be generated in the quantum dot devices **100**, and monitoring the result of those operations. For example, as discussed above, different quantum dots may be allowed to interact, the quantum states of different quantum dots may be set or transformed, and the quantum states of quantum dots may be read (e.g., by another quantum dot). The quantum processing device **2026** may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device **2026** may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device **2026** may also include support circuitry to support the processing capability of the quantum processing device **2026**, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0093] As noted above, the processing device **2002** may include a non-quantum processing device **2028**. In some embodiments, the non-quantum processing device **2028** may provide peripheral logic to support the operation of the quantum processing device **2026**. For example, the non-quantum processing device **2028** may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, control the performance of any of the operations discussed above with reference to FIGS. **6-8**, etc. The non-quantum processing device **2028** may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device **2026**. For example, the non-quantum processing device **2028** may interface with one or more of the other components of the quantum computing device **2000** (e.g., the communication chip **2012** discussed below, the display device **2006** discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device **2026** and conventional components. The non-quantum processing device **2028** may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0094] The quantum computing device **2000** may include a memory **2004**, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device **2026** may be read and stored in the memory **2004**. In some embodiments, the

memory **2004** may include memory that shares a die with the non-quantum processing device **2028**. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0095] The quantum computing device **2000** may include a cooling apparatus **2030**. The cooling apparatus **2030** may maintain the quantum processing device **2026** at a predetermined low temperature during operation to reduce the effects of scattering in the quantum processing device **2026**. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device **2028** (and various other components of the quantum computing device **2000**) may not be cooled by the cooling apparatus **2030**, and may instead operate at room temperature. The cooling apparatus **2030** may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0096] In some embodiments, the quantum computing device **2000** may include a communication chip **2012** (e.g., one or more communication chips). For example, the communication chip **2012** may be configured for managing wireless communications for the transfer of data to and from the quantum computing device **2000**. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0097] The communication chip **2012** may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip **2012** may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip **2012** may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip **2012** may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip **2012** may operate in accordance with other wireless protocols in other embodiments. The quantum computing device **2000** may include an antenna **2022** to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0098] In some embodiments, the communication chip **2012** may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip **2012** may include multiple communication chips. For instance, a first communication chip **2012** may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip **2012** may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip **2012** may be dedicated to wireless communications, and a second communication chip **2012** may be dedicated to wired communications.

[0099] The quantum computing device **2000** may include battery/power circuitry **2014**. The battery/power circuitry **2014** may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device **2000** to an energy source separate from the quantum computing device **2000** (e.g., AC line power).

[0100] The quantum computing device **2000** may include a display device **2006** (or corresponding interface circuitry, as discussed above). The display device **2006** may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0101] The quantum computing device **2000** may include an audio output device **2008** (or corresponding interface circuitry, as discussed above). The audio output device **2008** may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0102] The quantum computing device **2000** may include an audio input device **2024** (or corresponding interface circuitry, as discussed above). The audio input device **2024** may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0103] The quantum computing device **2000** may include a global positioning system (GPS) device **2018** (or corresponding interface circuitry, as discussed above). The GPS device **2018** may be in communication with a satellite-based system and may receive a location of the quantum computing device **2000**, as known in the art.

[0104] The quantum computing device **2000** may include an other output device **2010** (or corresponding interface circuitry, as discussed above). Examples of the other output device **2010** may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0105] The quantum computing device **2000** may include an other input device **2020** (or corresponding interface circuitry, as discussed above). Examples of the other input device **2020** may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0106] The quantum computing device **2000**, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0107] Any suitable materials may be used in various ones of the embodiments disclosed herein. For example, in some embodiments, the gate dielectric **114** may be a multilayer gate dielectric. The gate dielectric **114** may be, for example, silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric **114** may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate dielectric **114** may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric **114** to improve the quality of the gate dielectric **114**.

[0108] In some embodiments, any of the gate metals (e.g., the barrier gate metal **108** and/or the quantum dot gate metal **106**) may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. The spacer materials (e.g., the spacer material **118**, **134**, or **140**) may be any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride). The insulating materials **128** may include silicon oxide, silicon nitride, aluminum oxide, carbon-doped oxide, and/or silicon oxynitride, for example. Hardmasks (e.g., the hardmasks **110** and **112**) may be formed of silicon nitride, silicon carbide, or another suitable material.

[0109] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0110] Example A1 is a quantum dot device, including: a quantum well stack; a plurality of first gates above the quantum well stack; and a plurality of second gates above the quantum well stack; wherein a first gate is between each nearest neighbor pair of second gates.

[0111] Example A2 is a quantum dot device, including: a quantum well stack; a plurality of first gates above the quantum well stack; and a plurality of second gates above the quantum well stack; wherein the plurality of first gates are arranged in electrically continuous rows extending in a first direction, and the plurality of second gates are arranged in electrically continuous rows extending in a second direction perpendicular to the first direction.

[0112] Example A3 is a quantum dot device, including: a quantum well stack; a plurality of first gates above the quantum well stack; and a plurality of second gates above the quantum well stack; wherein the plurality of second gates are arranged as points in a grid, and diagonal subsets of the plurality of second gates with respect to the grid are electrically continuous.

[0113] Example A4 may include the subject matter of any of Examples A1-3, and may further specify that an individual first gate includes a first gate metal that extends between multiple nearest neighbor pairs of the second gates.

[0114] Example A5 may include the subject matter of any of Examples A1-4, and may further specify that an insulating material is disposed between a first one of the first gates and a second one of the first gates adjacent to the first one of the first gates.

[0115] Example A6 may include the subject matter of Example A5, and may further specify that at least one second gate is disposed between the first one of the first gates and a third one of the first gates adjacent to the first one of the first gates such that the first one of the first gates is between the second one of the first gates and the third one of the first gates.

[0116] Example A7 may include the subject matter of any of Examples A1-6, and may further include a hardmask above gate metal of the first gates.

[0117] Example A8 may include the subject matter of any of Examples A1-7, and may further include multiple hardmasks above gate metal of the first gates.

[0118] Example A9 may include the subject matter of Example A8, and may further include an insulating material between at least two of the hardmasks.

[0119] Example A10 may include the subject matter of any of Examples A7-9, and may further include an insulating material on the hardmask such that the insulating material is between the hardmask and gate metal of the second gates.

[0120] Example A11 may include the subject matter of any of Examples A1-10, and may further include insulating material between gate metal of the first gates and gate metal of the second gates such that the gate metal of the first gates is between the insulating material and the quantum well stack.

[0121] Example A12 may include the subject matter of any of Examples A1-11, and may further include spacer material between gate metal of the first gates and gate metal of the second gates.

[0122] Example A13 may include the subject matter of any of Examples A1-12, and may further include second gate metal stubs alternatingly arranged with second gates.

[0123] Example A14 may include the subject matter of any of Examples A1-13, and may further include spacer material disposed above gate metal of the second gates.

[0124] Example A15 may include the subject matter of any of Examples A1-14, and may further include a gate dielectric between gate metal of the first gates and the quantum well stack.

[0125] Example A16 may include the subject matter of Example A15, and may further specify that the gate dielectric continuously extends between gate metal of the second gates and the quantum well stack.

[0126] Example A17 may include the subject matter of any of Examples A1-16, and may further specify that the first gates are dimensioned and positioned in accordance with a pitch halving technique.

[0127] Example A18 may include the subject matter of any of Examples A1-17, and may further specify that the

second gates are dimensioned and positioned in accordance with a pitch halving technique.

[0128] Example A19 may include the subject matter of any of Examples A1-18, and may further include a multiplexer coupled to the first gates.

[0129] Example A20 may include the subject matter of Example A19, and may further specify that the multiplexer is a first multiplexer, and the quantum dot device further includes a multiplexer coupled to the second gates.

[0130] Example A21 may include the subject matter of any of Examples A1-20, and may further specify that the first gates have a pitch between 40 nanometers and 100 nanometers.

[0131] Example A22 may include the subject matter of any of Examples A1-21, and may further specify that the second gates have a pitch that is different from a pitch of the first gates.

[0132] Example A23 may include the subject matter of any of Examples A1-21, and may further specify that a pair of nearest neighbor second gates has a pitch between 60 nanometers and 100 nanometers.

[0133] Example A24 may include the subject matter of any of Examples A1-23, and may further include a plurality of parallel first gate lines extending away from the plurality of first gates.

[0134] Example A25 may include the subject matter of Example A24, and may further include a plurality of parallel second gate lines extending away from the plurality of second gates in a direction perpendicular to the first gate lines.

[0135] Example A26 may include the subject matter of any of Examples A1-25, and may further include a plurality of magnets disposed above the plurality of second gates.

[0136] Example A27 may include the subject matter of any of Examples A1-26, and may further specify that the first gates are barrier gates and the second gates are quantum dot gates.

[0137] Example B1 is a method of performing a Pauli gate operation with the quantum dot device of Example A27, including: applying voltages to the barrier gates and the quantum dot gates to form a quantum dot in the quantum well stack under a first quantum dot gate; and applying a microwave pulse to multiple quantum dot gates arranged in an electrically continuous row, wherein the multiple quantum dot gates include the first quantum dot gate, and wherein the microwave pulse is tuned to a frequency of a magnet disposed above the first quantum dot gate to perform a Pauli gate operation on the quantum dot.

[0138] Example B2 may include the subject matter of Example B1, and may further specify that voltages on the barrier gates are held constant while the microwave pulse is applied to the multiple quantum dot gates.

[0139] Example B3 may include the subject matter of any of Examples B1-2, and may further specify that voltages on other quantum dot gates are held constant while the microwave pulse is applied to the multiple quantum dot gates.

[0140] Example B4 may include the subject matter of any of Examples B1-3, and may further specify that the quantum dot is an electron spin quantum dot.

[0141] Example C1 is a method of performing an exchange gate operation with the quantum dot device of Example A27, including: applying voltages to the barrier gates and the quantum dot gates to form a first quantum dot in the quantum well stack under a first quantum dot gate and to form a second quantum dot in the quantum well stack under a second quantum dot gate, wherein the first quantum dot gate is included in a first plurality of quantum dot gates that are arranged in an electrically continuous row, the second quantum dot gate is included in a second plurality of quantum dot gates that are arranged in an electrically continuous row, and a first barrier gate is disposed between the first quantum dot gate and the second quantum dot gate; providing off voltages to the plurality of barrier gates; applying a first set of mutually tuning voltages to the first plurality of quantum dot gates and to first additional pluralities of quantum dot gates arranged in additional electrically continuous rows to one side of the first plurality of quantum dot gate in a first direction; applying a second set of mutually tuning voltages to the second plurality of quantum dot gate and to second additional pluralities of quantum dot gates arranged in additional electrically continuous rows to one side of the second plurality of quantum dot gates in a second direction opposite to the first direction, wherein the first plurality of quantum dot gates and the second plurality of quantum dot gates are detuned; and lowering the energy barrier on the first barrier gate relative to the other barrier gates to allow the first and second quantum dots to interact.

[0142] Example C2 may include the subject matter of Example C1, and may further specify that lowering the energy barrier includes increasing the voltage on the first barrier gate.

[0143] Example D1 is a method of manufacturing a quantum dot device, including: providing a plurality of first gate metal rows above a quantum well stack, wherein individual ones of the plurality of first gate metal rows are oriented in a first direction; providing an insulating material above the plurality of first gate metal rows; and providing a plurality of second gate metal rows above the insulating material, wherein individual ones of the plurality of second gate metal rows are oriented in a second direction perpendicular to the first direction, and the second gate metal extends down between at least some adjacent pairs of first gate metal rows.

[0144] Example D2 may include the subject matter of Example D1, and may further specify that the plurality of first gate metal rows are provided on a layer of gate dielectric on the quantum well stack.

[0145] Example D3 may include the subject matter of Example D2, and may further specify that the second gate metal extends down between at least some adjacent pairs of first gate metal rows to contact the gate dielectric.

[0146] Example D4 may include the subject matter of any of Examples D1-3, and may further specify that providing the plurality of first gate metal rows includes patterning the first gate metal rows by pitch halving.

[0147] Example D5 may include the subject matter of any of Examples D1-4, and may further specify that providing the plurality of second gate metal rows includes patterning the second gate metal rows by pitch halving.

[0148] Example D6 may include the subject matter of any of Examples D1-5, and may further specify that the insulating material includes a hardmask.

[0149] Example D7 may include the subject matter of any of Examples D1-6, and may further specify that the insulating material includes an interlayer dielectric.

[0150] Example D8 may include the subject matter of any of Examples D1-7, and may further include providing spacer material on side faces of the first gate metal rows.

[0151] Example D9 may include the subject matter of any of Examples D1-8, and may further include providing spacer material on side faces of the second gate metal rows.

[0152] Example E1 is a quantum computing device, including: a quantum processing device, wherein the quantum processing device includes the quantum dot device of any of Examples A1-27; a non-quantum processing device, coupled to the quantum processing device, to control electrical signals applied to the first and second gates; and a memory device to store data generated during operation of the quantum processing device.

[0153] Example E2 may include the subject matter of Example E1, and may further include a cooling apparatus to maintain the temperature of the quantum processing device below 5 degrees Kelvin.

[0154] Example E3 may include the subject matter of Example E2, and may further specify that the cooling apparatus includes a dilution refrigerator.

[0155] Example E4 may include the subject matter of Example E2, and may further specify that the cooling apparatus includes a liquid helium refrigerator.

[0156] Example E5 may include the subject matter of any of Examples E1-4, and may further specify that the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

1. A quantum dot device, comprising:
a quantum well stack;
an insulating material over the quantum well stack;
openings in the insulating material, the openings arranged along a direction and extending to the quantum well stack; and
a gate metal at least partially filling the openings.

2. The quantum dot device of claim **1**, further comprising a gate dielectric separating the gate metal in the openings and the quantum well stack.

3. The quantum dot device of claim **2**, wherein the gate dielectric in different ones of the openings are portions of a materially continuous layer of the gate dielectric.

4. The quantum dot device of claim **3**, wherein the materially continuous layer of the gate dielectric is further on sidewalls of the openings.

5. The quantum dot device of claim **2**, further comprising the gate metal over the insulating material, between the openings, materially continuous with the gate metal at least partially filling the openings.

6. The quantum dot device of claim **1**, further comprising the gate metal over the insulating material, between the openings, materially continuous with the gate metal at least partially filling the openings.

7. The quantum dot device of claim **6**, wherein the gate metal over the insulating material is a line of the gate metal, extending along the direction.

8. The quantum dot device of claim **7**, wherein the openings are first openings, the direction is a first direction, the gate metal is a first gate metal, and the quantum dot device further includes:
second openings in the insulating material, the second openings arranged along a second direction and extending to the quantum well stack, the second direction being parallel to the first direction; and
a second gate metal at least partially filling the second openings.

9. The quantum dot device of claim **8**, further comprising the second gate metal over the insulating material, between the second openings, materially continuous with the second gate metal at least partially filling the second openings, wherein the second gate metal over the insulating material is a line of the second gate metal, extending along the second direction.

10. The quantum dot device of claim **8**, wherein a center-to-center distance between one of the first openings and one of the second openings is smaller than a center-to-center distance between closest two of the first openings.

11. The quantum dot device of claim **6**, further comprising a further gate metal, wherein the further gate metal is between the quantum well stack and the gate metal over the insulating material.

12. The quantum dot device of claim **11**, wherein the further gate metal is electrically isolated from the gate metal.

13. The quantum dot device of claim **11**, wherein the direction is a first direction, and the further gate metal is a line of the further gate metal, extending along a second direction, the second direction being perpendicular to the first direction.

14. The quantum dot device of claim **13**, further comprising a gate dielectric between the line of the further gate metal and the quantum well stack.

15. The quantum dot device of claim **1**, wherein a center-to-center distance between adjacent ones of the openings is between 80 and 200 nanometers.

16. The quantum dot device of claim **1**, wherein the quantum dot device is a quantum computing device that includes:
a quantum processing device, comprising the quantum well stack, the insulating material, the openings, and the gate metal,
a non-quantum processing device, coupled to the quantum processing device, to control electrical signals applied to the gate metal at least partially filling the openings, and
a memory device to store data generated during operation of the quantum processing device.

17. A quantum dot device, comprising:
a quantum well stack;
first gates above the quantum well stack; and
second gates above the quantum well stack,
wherein the first gates are arranged in an electrically continuous row extending in a first direction, and the second gates are arranged in an electrically continuous row extending in a second direction perpendicular to the first direction.

18. The quantum dot device of claim **17**, further comprising an insulator material between the electrically continuous row extending in the first direction and the electrically continuous row extending in the second direction.

19. A quantum dot device, comprising:
a quantum well stack;
an insulating material over the quantum well stack;
a first opening and a second opening in the insulating material, extending to the quantum well stack; and
a gate metal having a first portion at least partially filling the first opening, a second portion at least partially filling the second opening, and a third portion above the insulating material and materially continuous with the first portion and the second portion.

20. The quantum dot device of claim **19**, further comprising:
a first line of a further gate metal; and
a second line of the further gate metal, wherein the first line and the second line are parallel, a projection of a line between the first opening and the second opening onto the quantum well stack is perpendicular to a projection of the first line onto the quantum well stack, and the first

line and the second line have portions under the third portion of the gate metal.

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